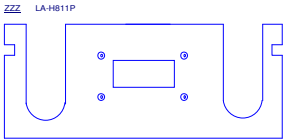


MODEL NAME : *Modena*
PCB NO : *LA-H811P*
BOM P/N : *451AHT31L01 ~ L32*



Dell/Compal Confidential

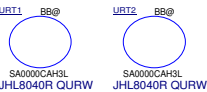
Schematic Document

(MODENA ICE Lake U)

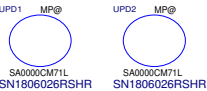
CPU Option



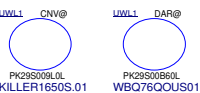
TBT Option



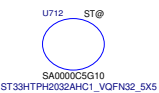
PD Option



WLAN Option



TPM Option



EC Option



2019-12-16
Rev: 1.0 (A00)

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Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 1%	4700p	X00	0.1
1	130K +/- 5%	4700p	X01	0.2
2	62K +/- 5%	4700p	X02	0.3
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p	N/A	N/A

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	VCCIN Controller	PD Controller	MIP160	USB/I2C MUX	BurnSide Bridge	Accel	TI Amp.
PCH_SML0CLK PCH_SML0DATA	PCH								Reserve		
PCH_SML1CLK PCH_SML1DATA	PCH					V			V		
SMBCLK SMBDATA	PCH						V				
EC_SMB03_CLK EC_SMB03_DAT	MECS106	V									
EC_SMB04_CLK EC_SMB04_DAT	MECS106					V		V			
EC_SMB05_CLK EC_SMB05_DAT	MECS106				Reserve						
EC_SMB10_CLK EC_SMB10_DAT	MECS106		V	V							
EC_SMB00_CLK EC_SMB00_DAT	MECS106									V	
EC_SMB01_CLK EC_SMB01_DAT	MECS106										V

Check

PCIE/USB3.1

Flexible I/O	Interface	DESTINATION
0	PCI-E#1 / USB 3.1#1	None
1	PCI-E#2 / USB 3.1#2	USB DCI Debug
2	PCI-E#3 / USB 3.1#3	WLAN PCIe Gen2
3	PCI-E#4 / USB 3.1#4	None
4	PCI-E#5 / USB 3.1#5	None
5	PCI-E#6 / USB 3.1#6	None
6	PCI-E#7	None
7	PCI-E#8	None
8	PCI-E#9	M.2 SSD
9	PCI-E#10	
10	PCI-E#11 / SATA#0	
11	PCI-E#12 / SATA#1a	
12	PCI-E#13	None
13	PCI-E#14	None
14	PCI-E#15 / SATA#1b	None
15	PCI-E#16 / SATA#2	Card Reader PCIE GEN2

USB 2.0

USB 2.0 PORT#	DESTINATION
1	USB DCI Debug
2	None
3	None
4	Type-C_R
5	FPR
6	None
7	None
8	Type-C_L
9	CAM
10	BT

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	WLAN
	CLKOUT_PCIE1	M.2 SSD
	CLKOUT_PCIE2	None
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Thunderbolt

	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None

Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

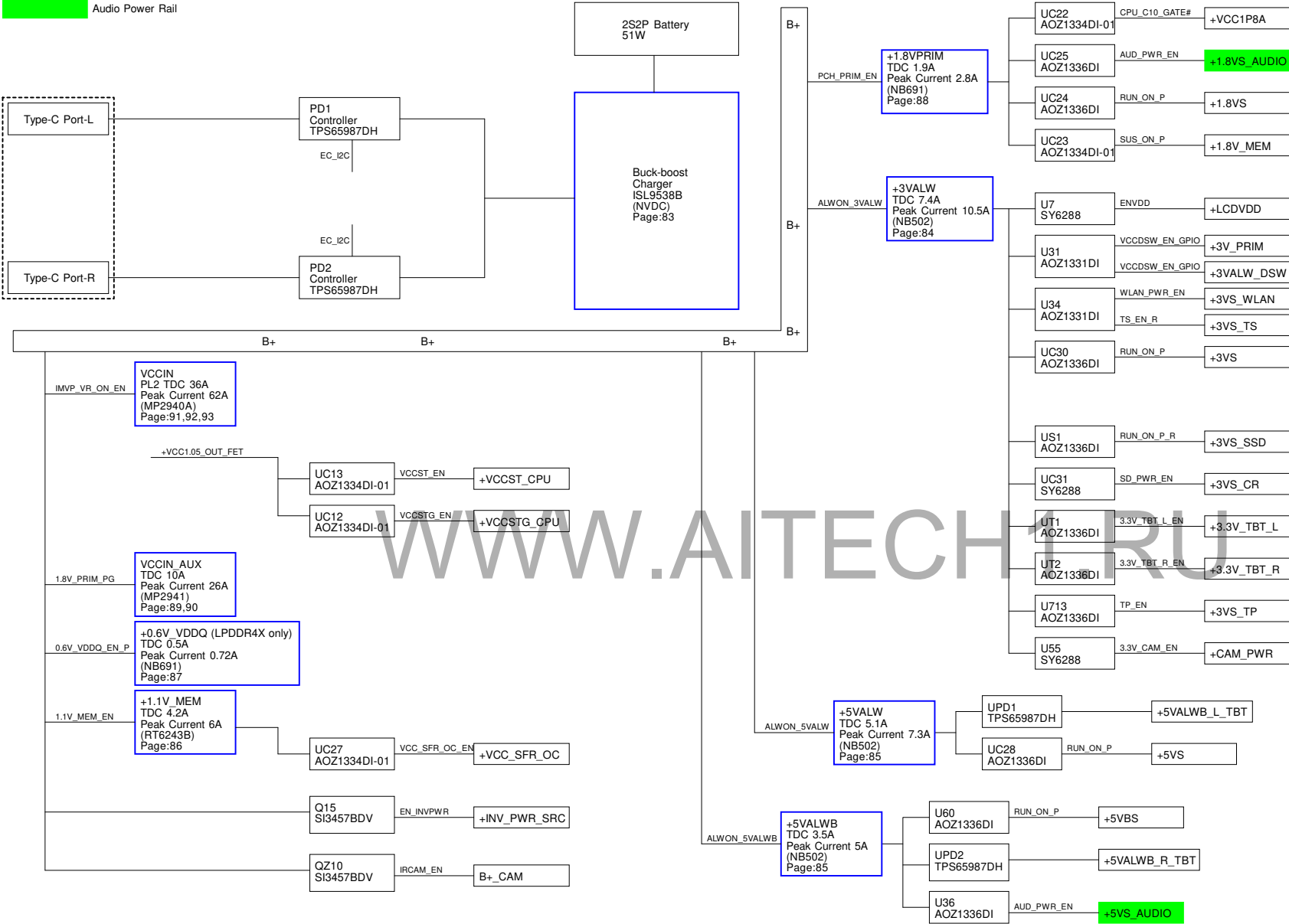
⏏ : means Analog Ground

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Modena POWER BLOCK DIAGRAM

Power Rail

Audio Power Rail



Power On Sequence

[AC in]

[Battery only, AC absent]

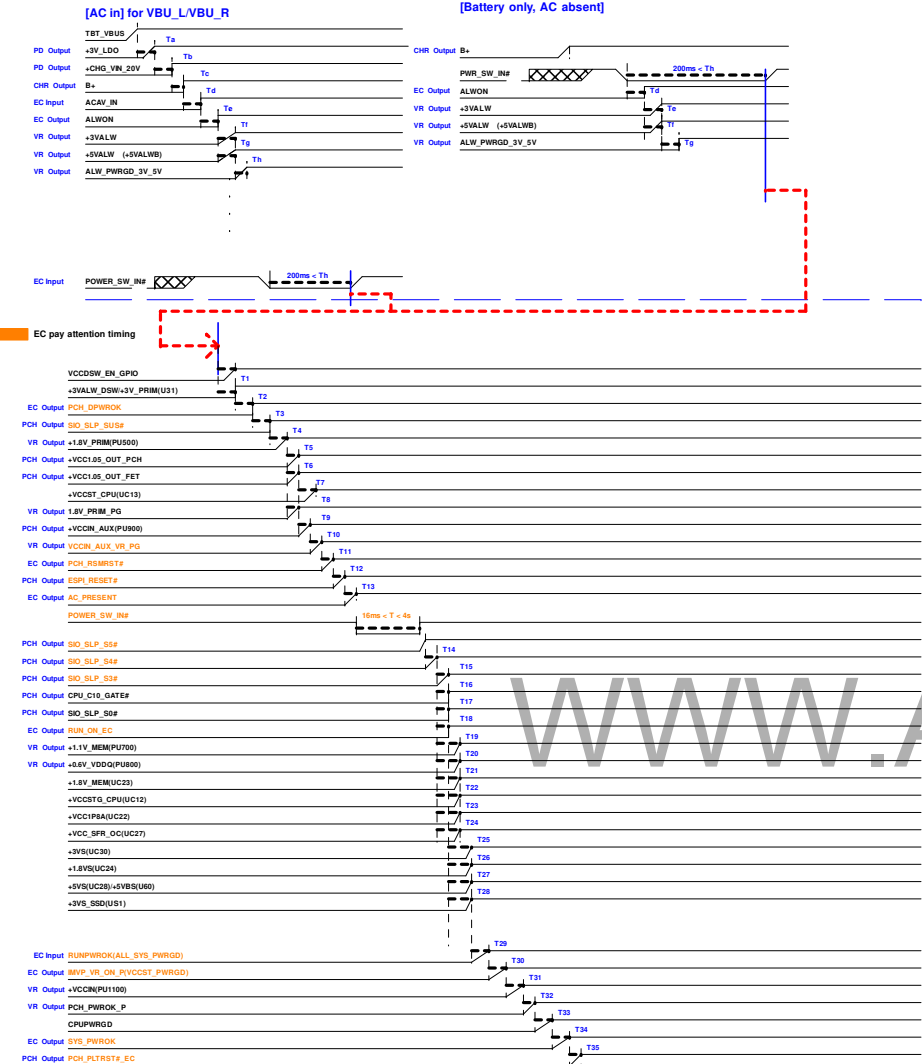
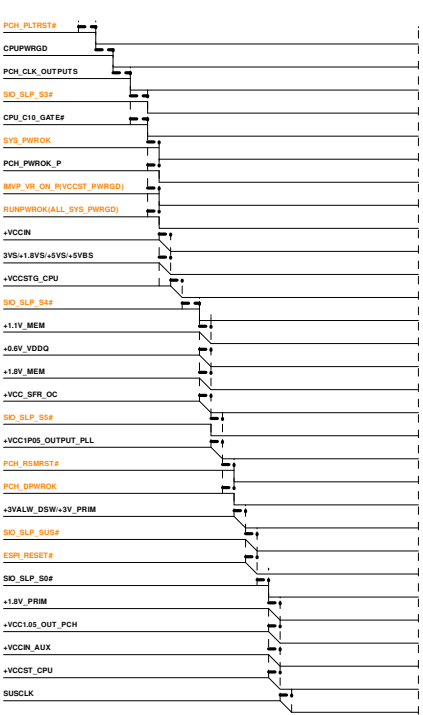
ITEM	Measure Point	Time
Ta	TBT_VBUS	To -3V_LDO
Tb	+3V_LDO	To -3V_LDO
Tc	+CHG_VIN_20V	To -CHG_VIN_20V
Td	B+	To ACAP_IN
Te	ACAP_IN	To ALWON
Tf	ALWON	To -3VALW
Tg	ALWON	To -3VALW (+5VALWB)
Th	-3VALW	To ALW_PWRGD_3V_5V
Ti	ALW_PWRGD_3V_5V	
Tj		
Tk		
Tl		
Tm		
Tn		
To		

ITEM	Measure Point	Time
Ta	TBT_VBUS	To -3V_LDO
Tb	+3V_LDO	To -3V_LDO
Tc	+CHG_VIN_20V	To -CHG_VIN_20V
Td	B+	To ACAP_IN
Te	ACAP_IN	To ALWON
Tf	ALWON	To -3VALW
Tg	ALWON	To -3VALW (+5VALWB)
Th	-3VALW	To ALW_PWRGD_3V_5V
Ti	ALW_PWRGD_3V_5V	
Tj		
Tk		
Tl		
Tm		
Tn		
To		

ITEM	Measure Point	Time
T1	VCCDSW_EN_GPI0	To -3VALW_DSW+3V_PRIM
T2	-3VALW_DSW+3V_PRIM	To PCH_DPWR0K
T3	PCH_DPWR0K	To SIO_SLP_S54#
T4	SIO_SLP_S54#	To +1.8V_PRIM
T5	+1.8V_PRIM	To +VCC1.05_OUT_PCH
T6	+1.8V_PRIM	To +VCC1.05_OUT_FET
T7	+VCC1.05_OUT_FET	To +VCCST_CPU
T8	+1.8V_PRIM	To 1.8V_PRIM_PG
T9	1.8V_PRIM_PG	To +VCCIN_AUX
T10	+VCCIN_AUX	To +VCCIN_AUX_VR_PG
T11	+VCCIN_AUX_VR_PG	To PCH_RSMRST#
T12	PCH_RSMRST#	To ESP_RESET#
T13	ESP_RESET#	To AC_PRESENT
T14	SIO_SLP_S54#	To SIO_SLP_S54#
T15	SIO_SLP_S54#	To SIO_SLP_S54#
T16	SIO_SLP_S54#	To CPU_C10_GATE#
T17	SIO_SLP_S54#	To SIO_SLP_S54#
T18	SIO_SLP_S54#	To RUN_ON_EC
T19	SIO_SLP_S54#	To +1.1V_MEM
T20	SIO_SLP_S54#	To +0.6V_VDDQ
T21	SIO_SLP_S54#	To +1.8V_MEM
T22	SIO_SLP_S54#	To +1.8V_MEM
T23	SIO_SLP_S54#	To +VCC1P0A
T24	SIO_SLP_S54#	To +VCC_SFR_OC
T25	RUN_ON_EC	To +3VS
T26	RUN_ON_EC	To +1.8VS
T27	RUN_ON_EC	To +3VS+5VS
T28	RUN_ON_EC	To +3VS+5VS
T29	RUN_ON_EC	To -SSD_PWR02
T30	RUN_ON_EC	To -SSD_PWR03
T31	-3VS	To RUNPWR0K
T32	RUNPWR0K	To BVP_VR_ON_PVCCST_PWRGD
T33	BVP_VR_ON_PVCCST_PWRGD	To +VCCIN
T34	+VCCIN	To PCH_PWR0K_P
T35	PCH_PWR0K_P	To CPU_PWR0D
T36	CPU_PWR0D	To SYS_PWR0K
T37	SYS_PWR0K	To PCH_PLTRST#_EC

Power Down Sequence

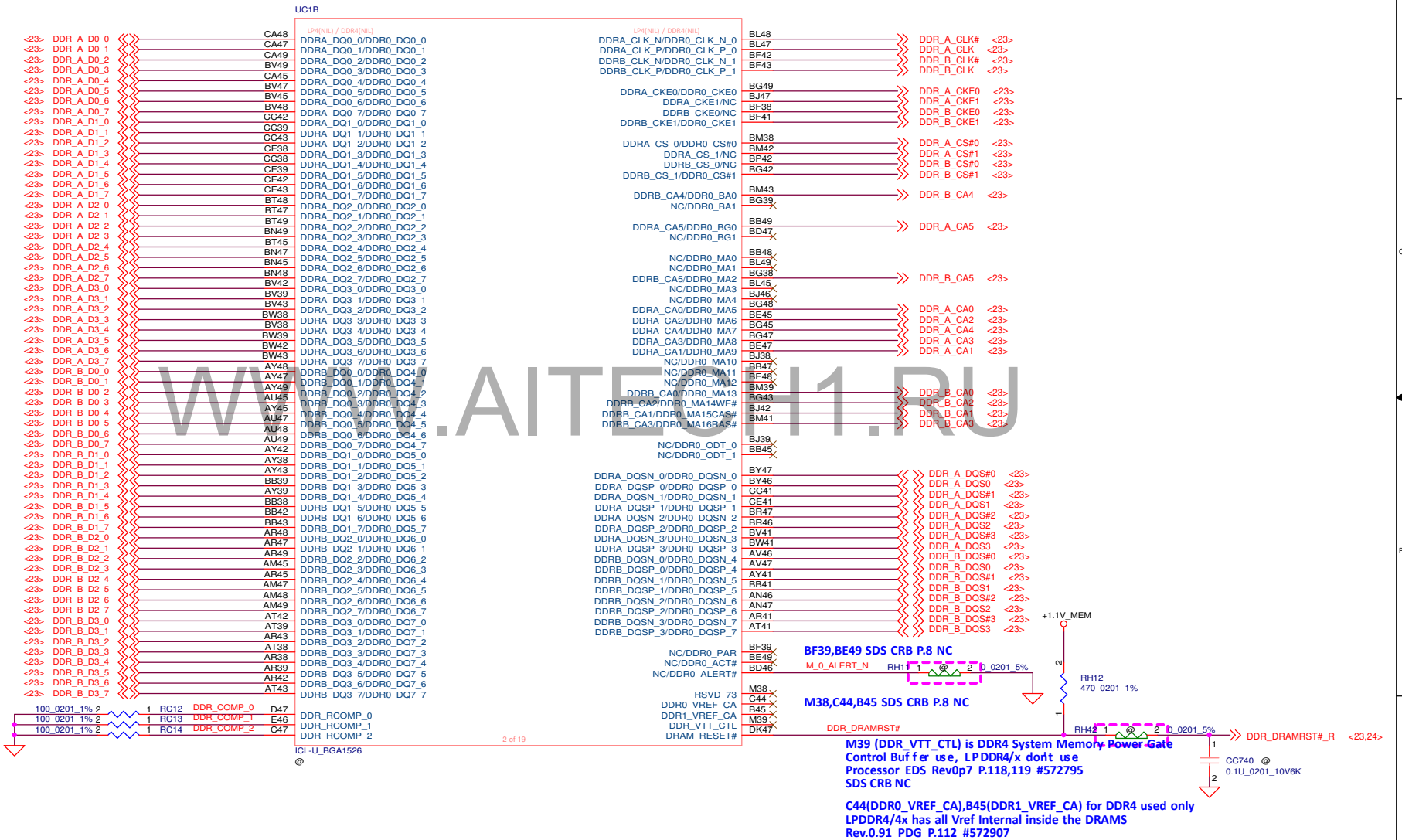
EC pay attention timing



EC pay attention timing

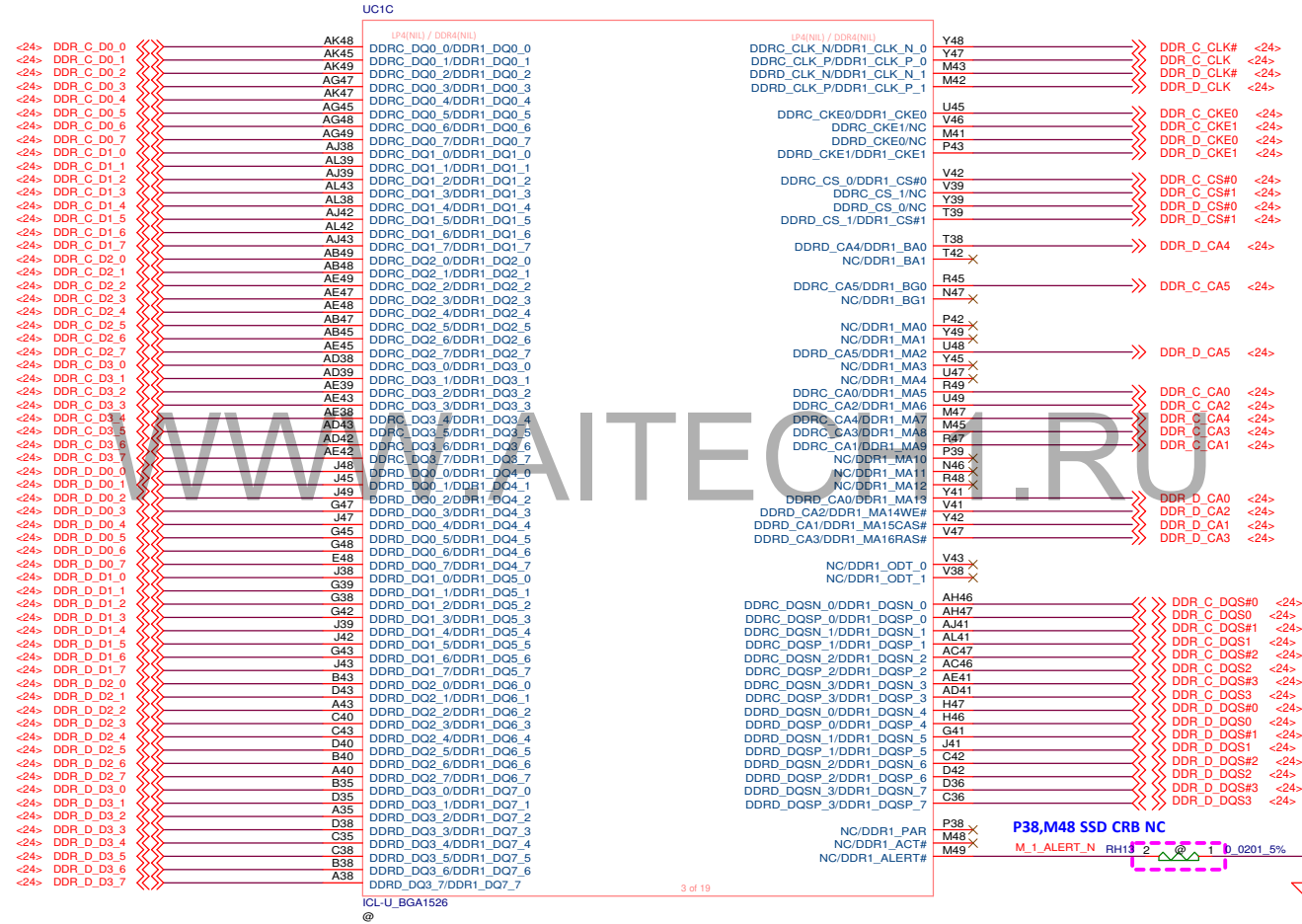
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Memory connection refer 573975 Rev1P1

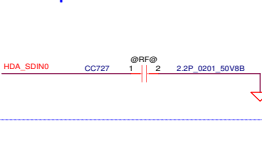
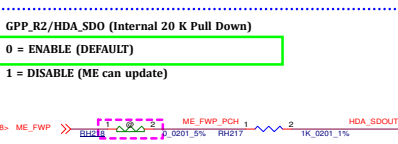
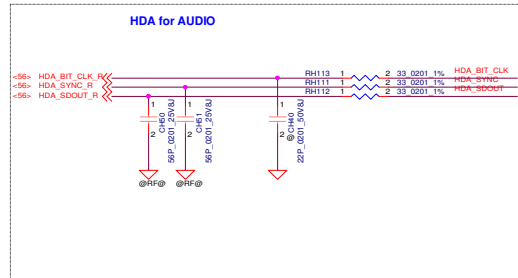
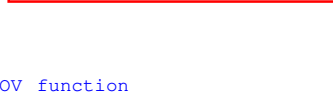
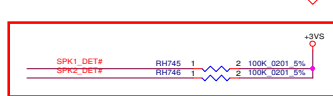
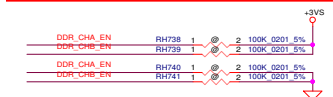
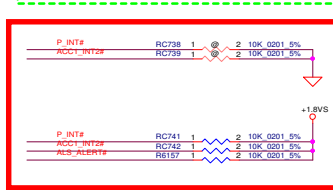
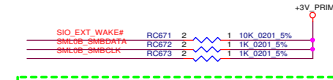
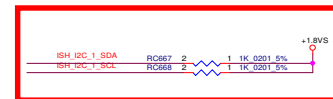


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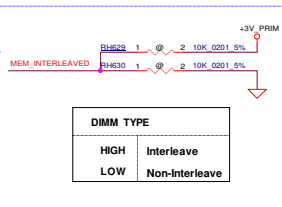
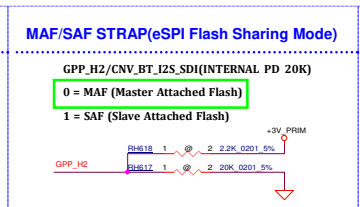
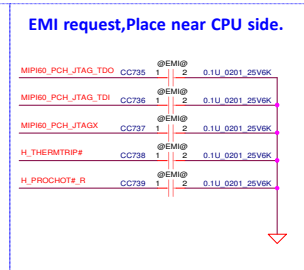
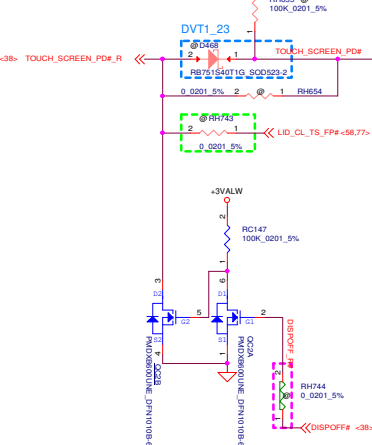
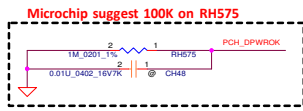
Memory connection refer 573975 Rev1P1



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PCIe SSDX4
PCIe Gen3

CardreaderX1
PCIe Gen2

USB debug

WLAN

USB debug

Type-C_R
FPR

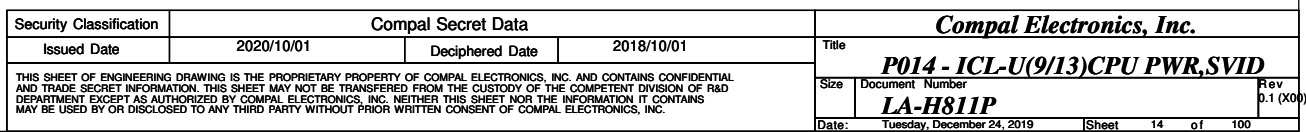
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UF Camera

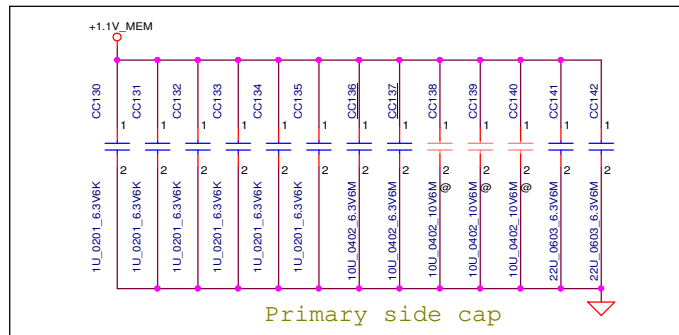
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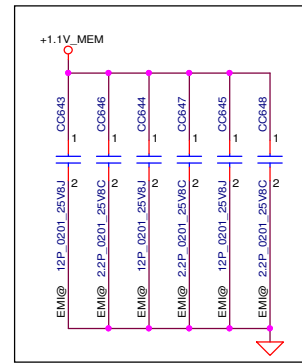


SVID DATA

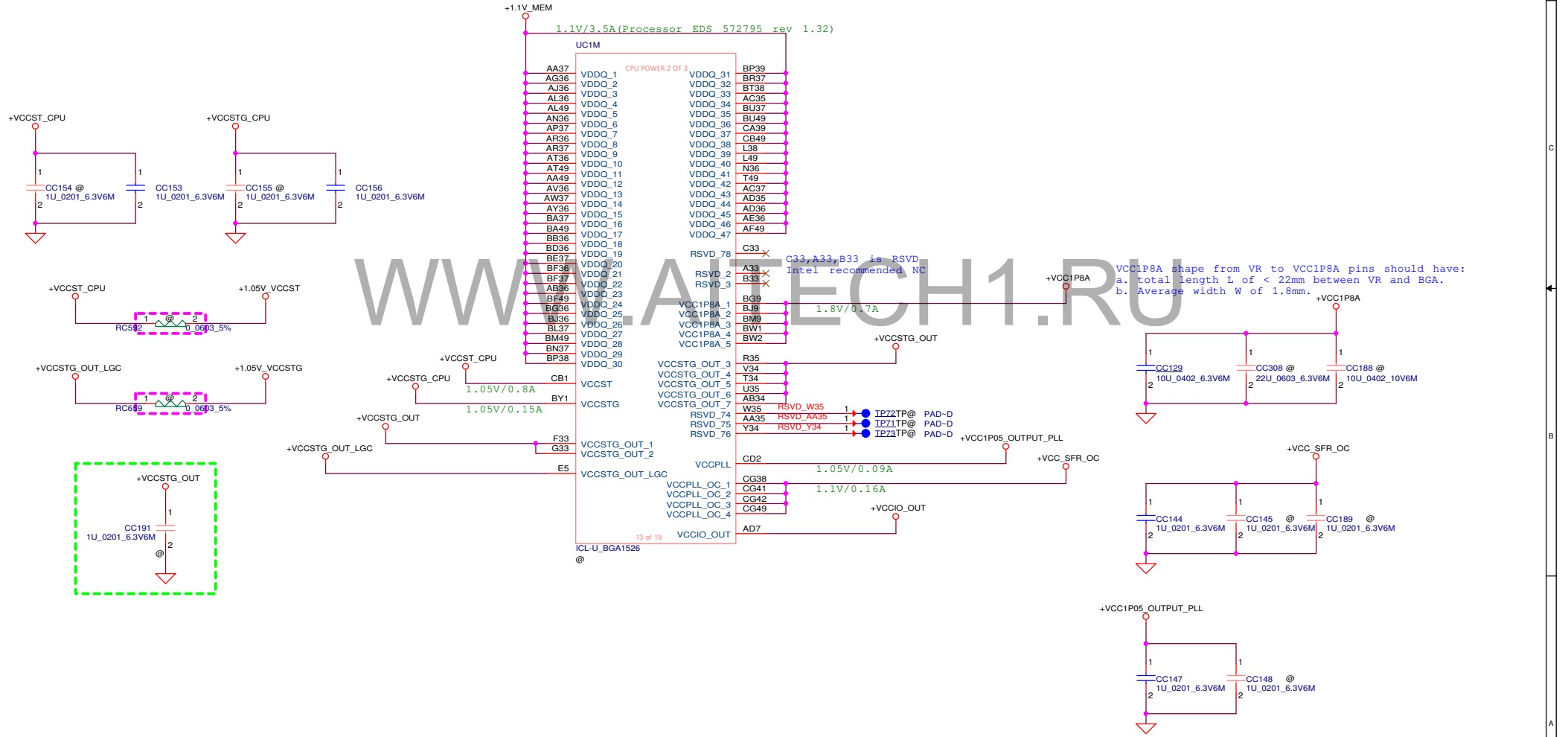
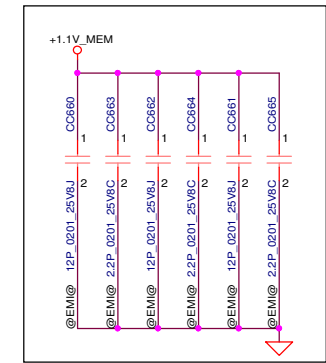




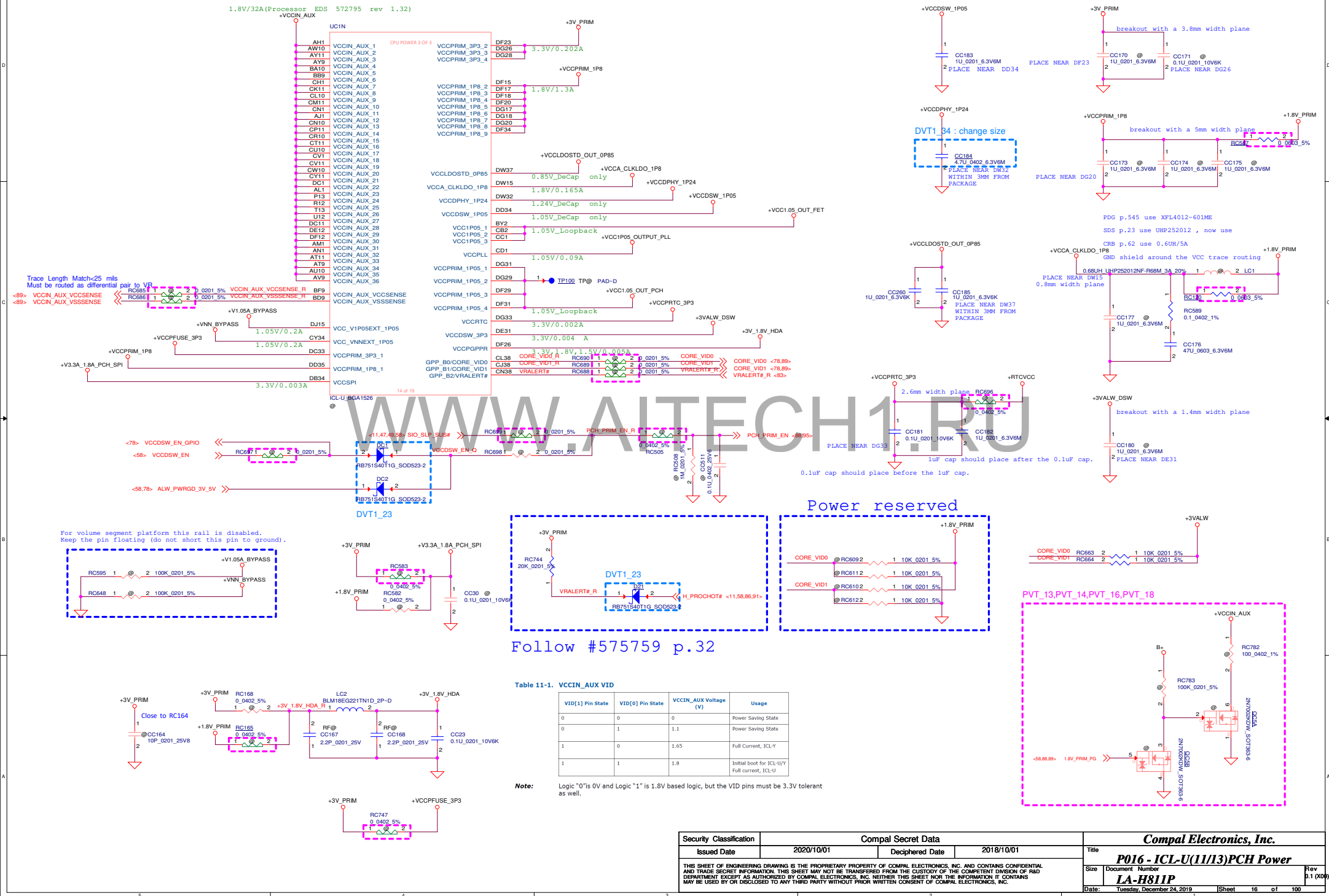
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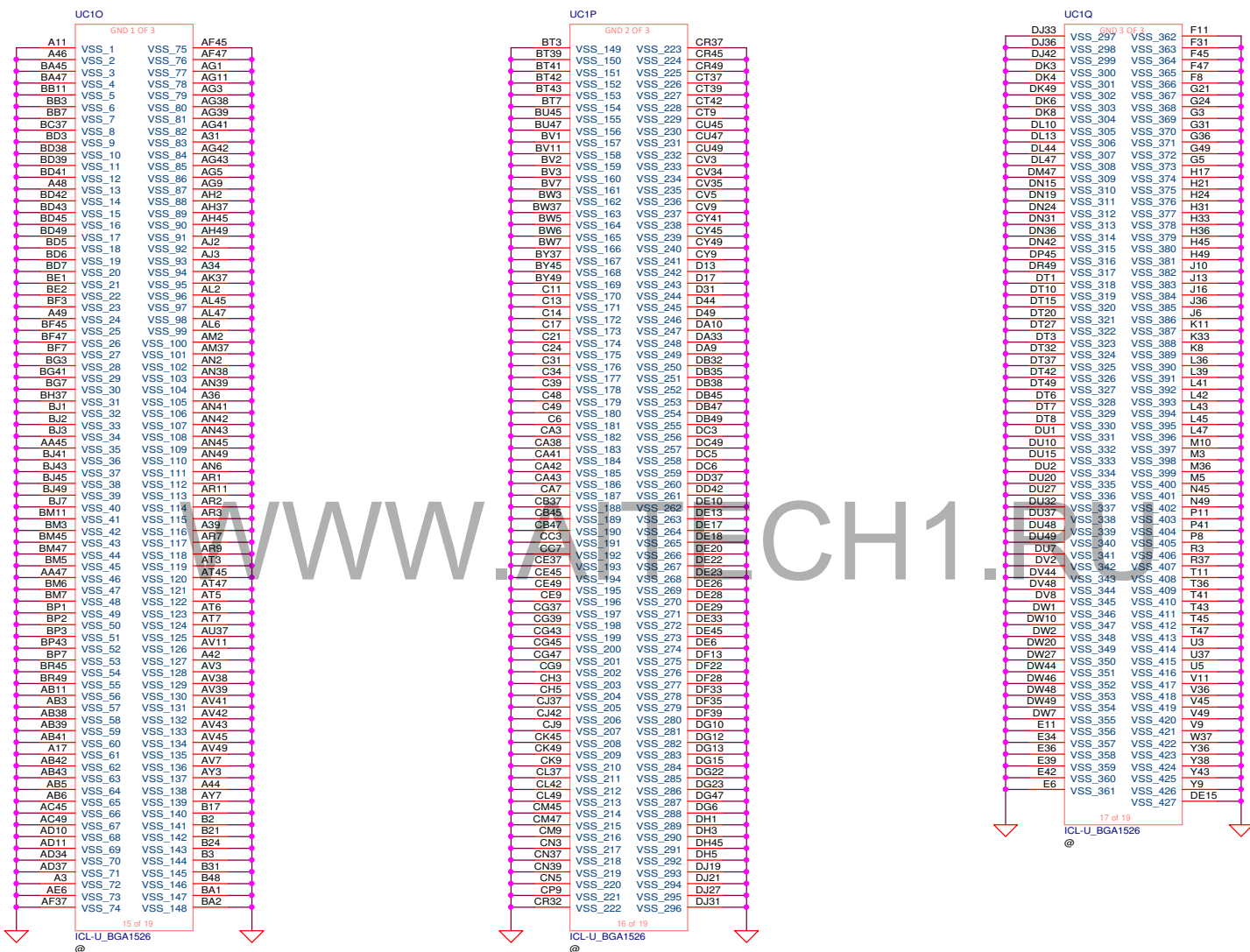


EMC CAPS
PLACE <160mil FROM SOC VDDQ,
WITH EACH PAIR <470mil APART

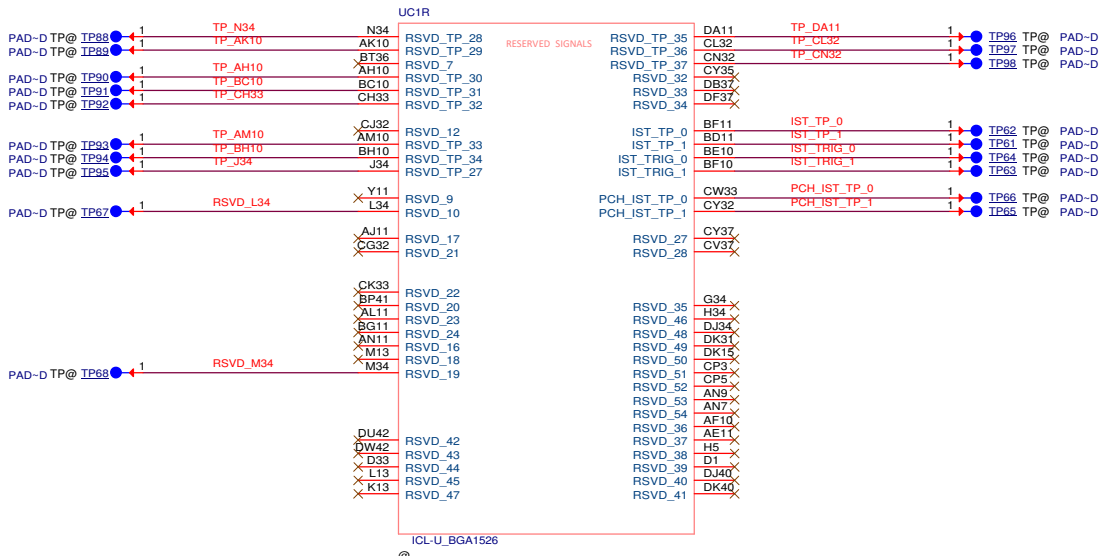
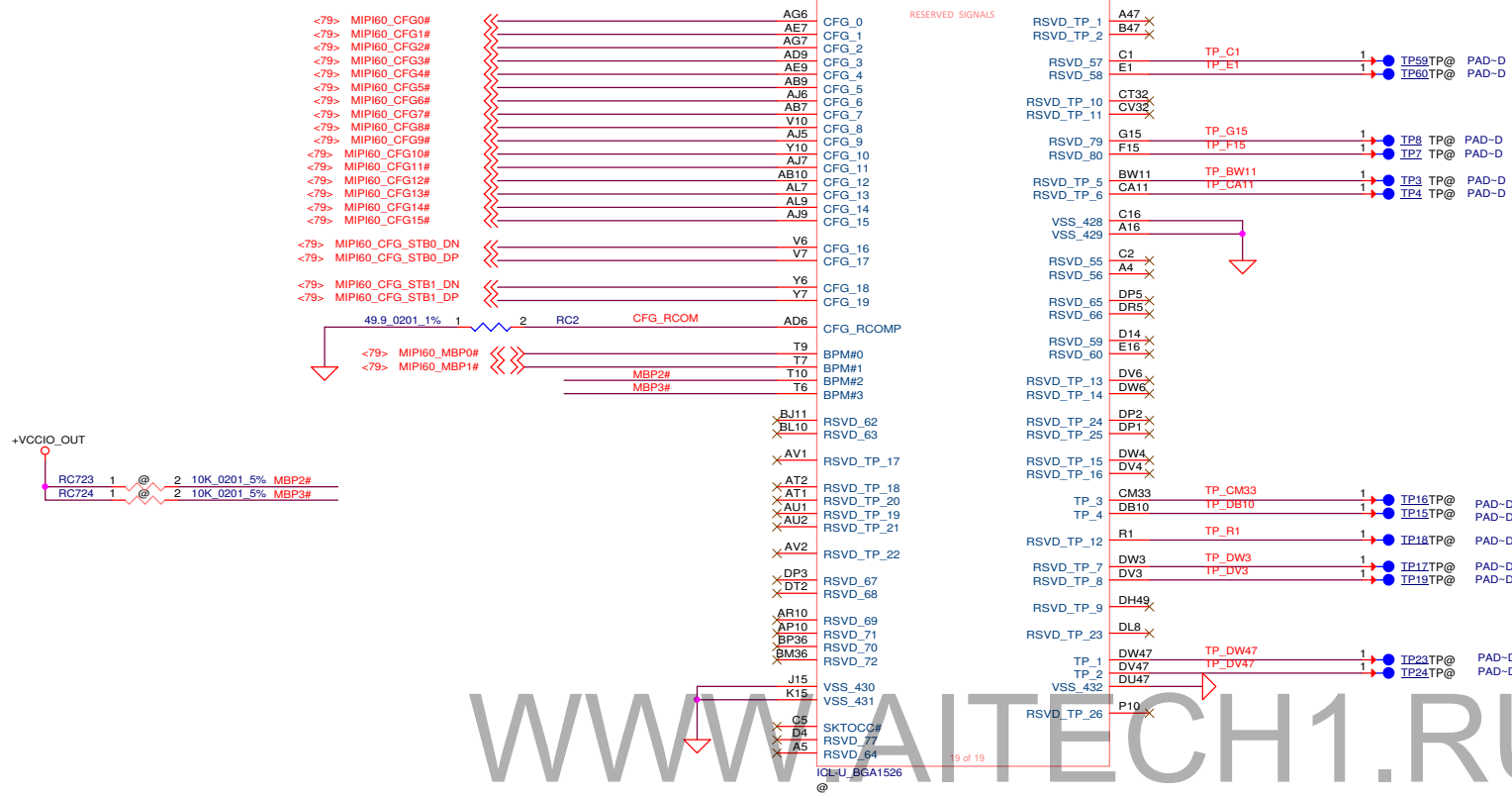


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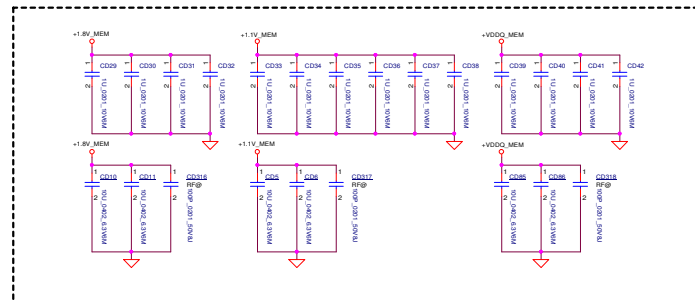
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Memory connection refer 573975 Rev1P1

DDRC



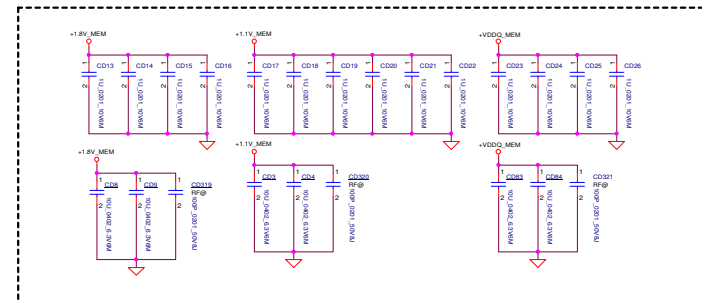
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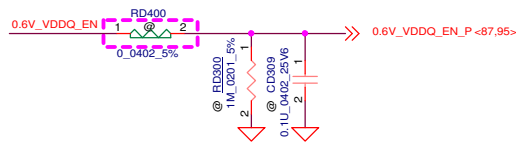
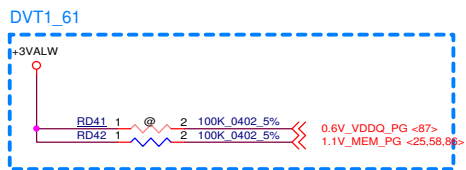
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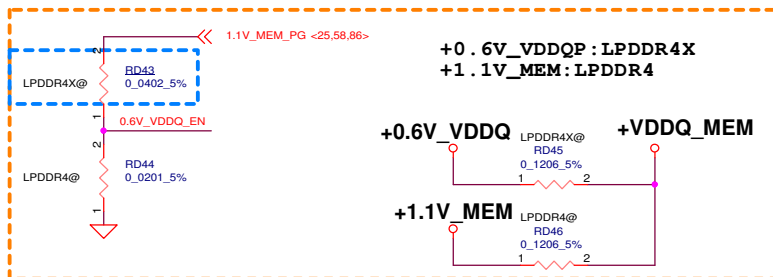
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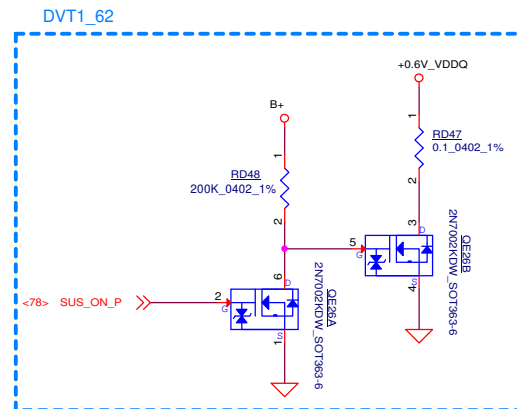
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DVT1_60



	RD43	RD45	RD44	RD46
LPDDR4 (1.1V) :	@	@		
LPDDR4X (1.1V&0.6V) :			@	@



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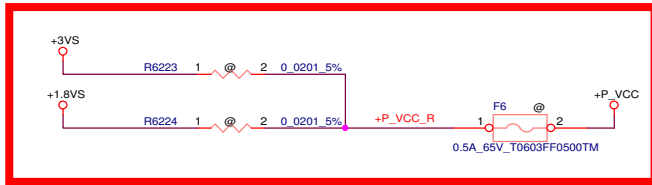
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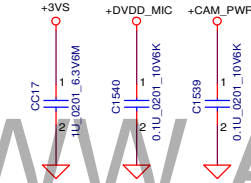
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For factory test request

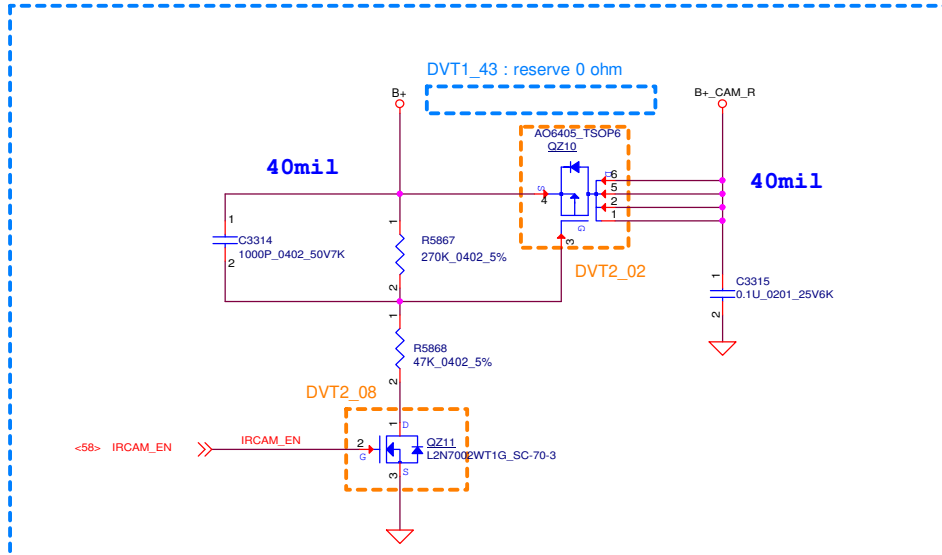
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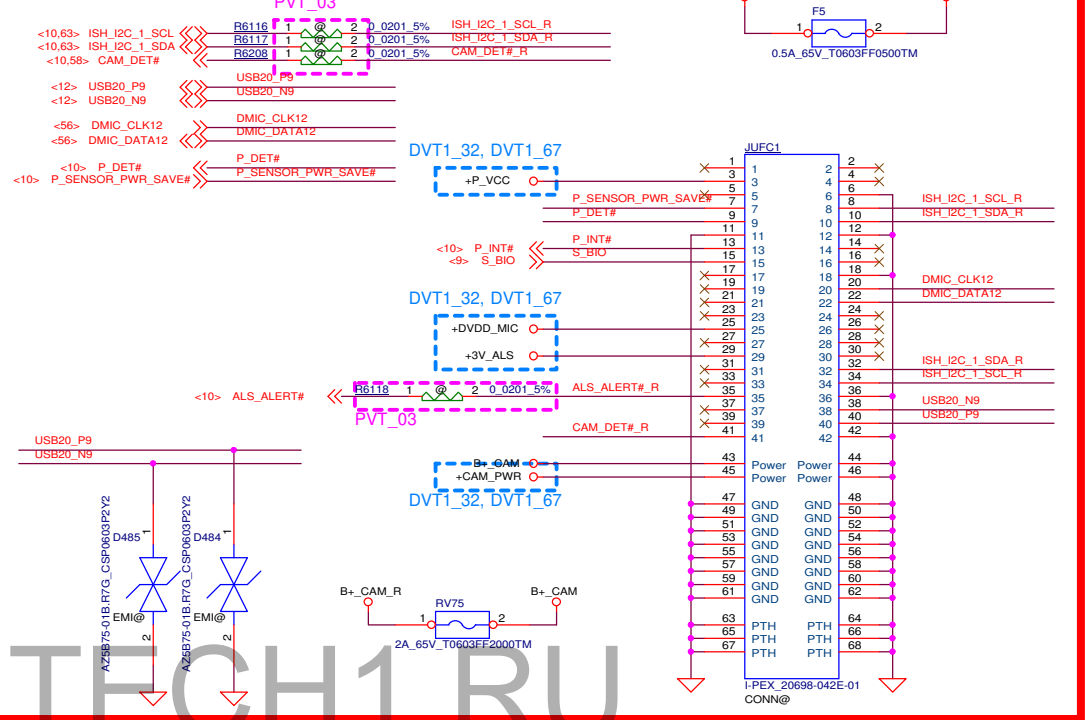
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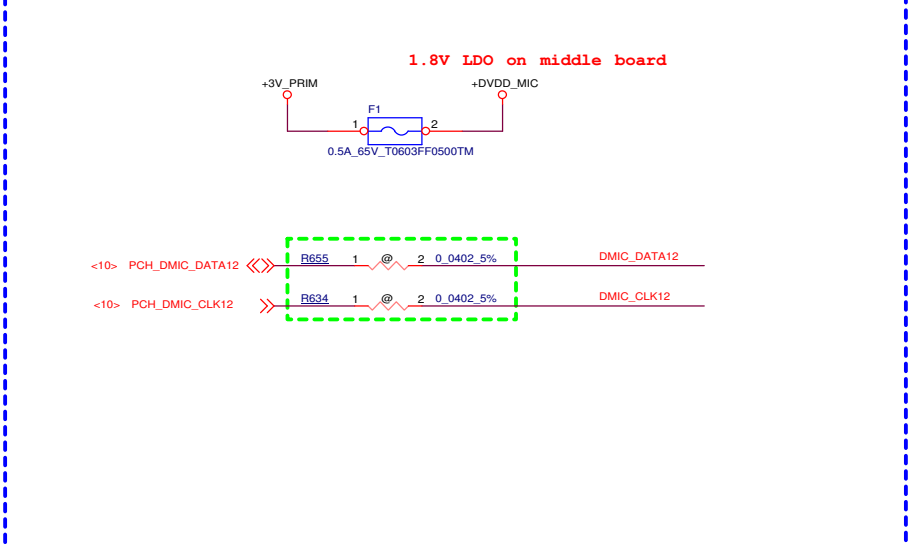
DVT1_20, DVT1_67



Camera, ALS, DMIC



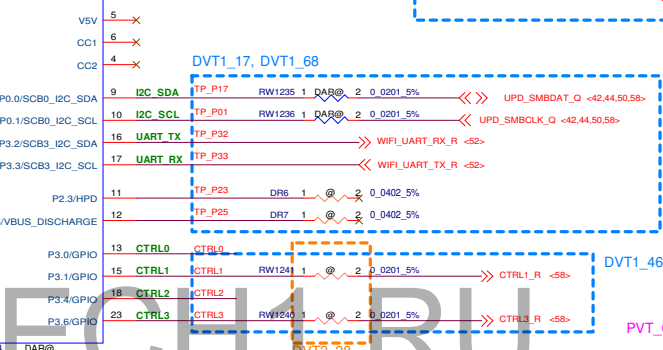
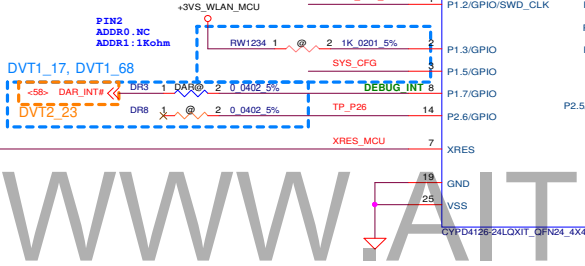
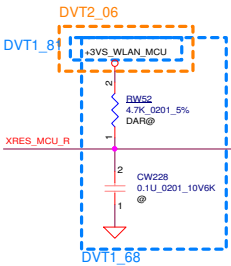
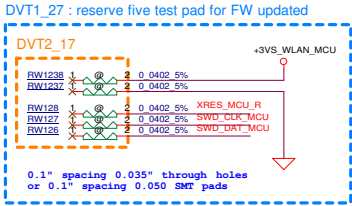
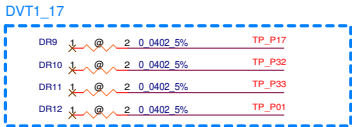
Intel DMIC for WOV function



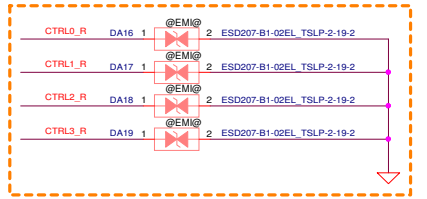
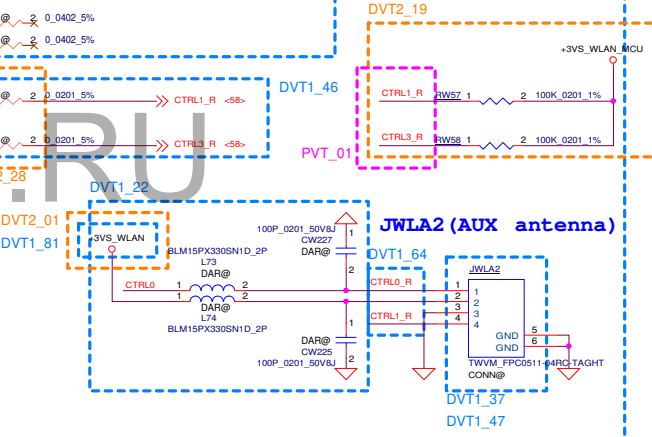
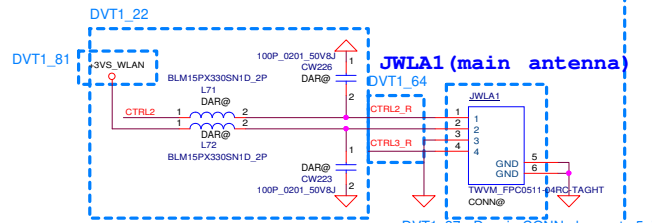
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Darwin 2.0

DVT1_16 : add Darwin2.0



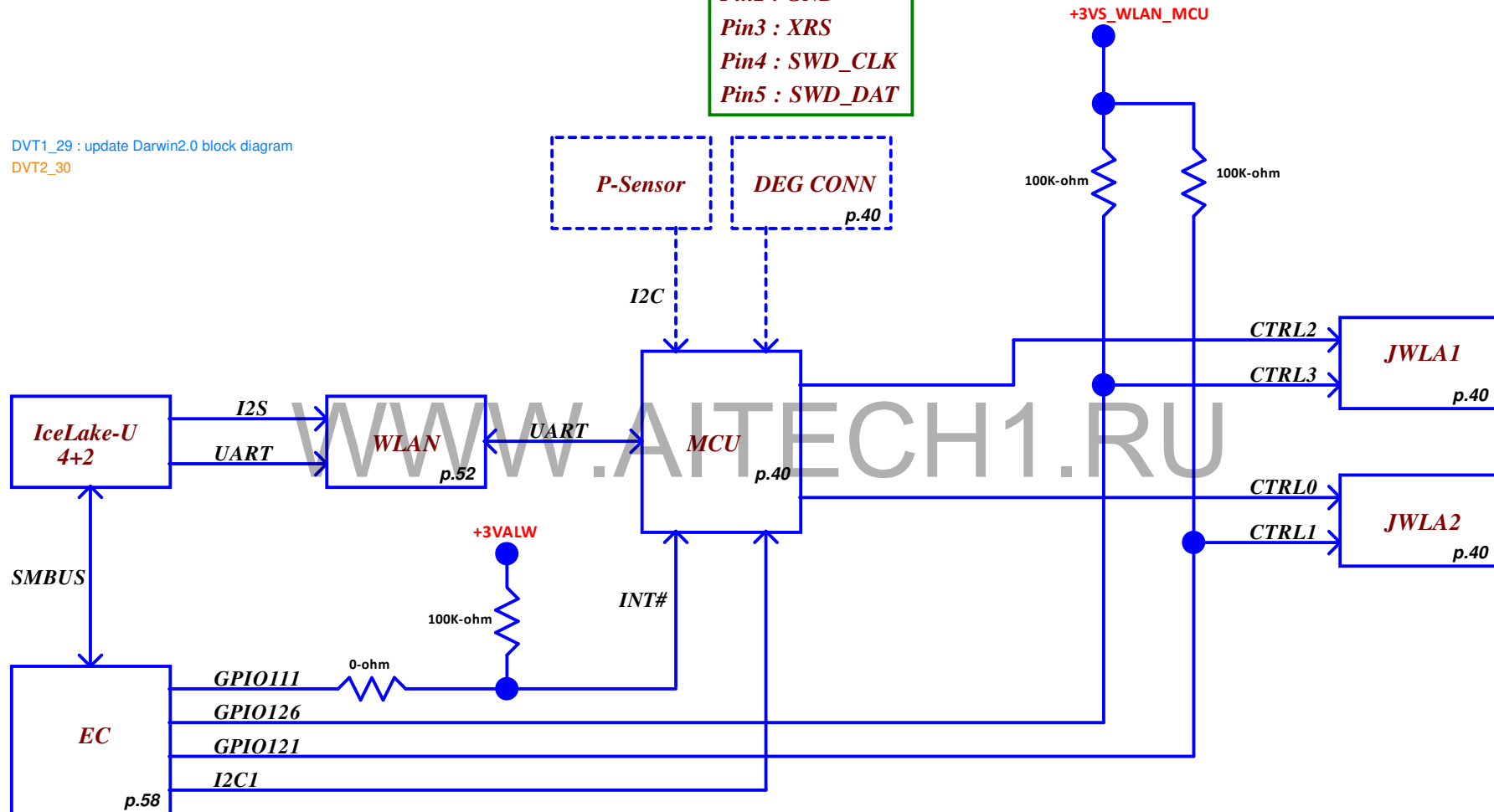
I2C ADDR	I2C Slave Address
NC	0x72 (default)
Pull up 3.3V	0x34



Pin definition

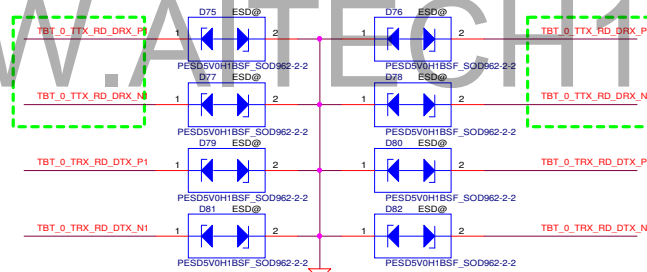
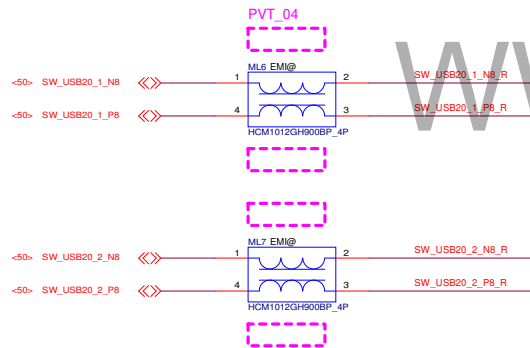
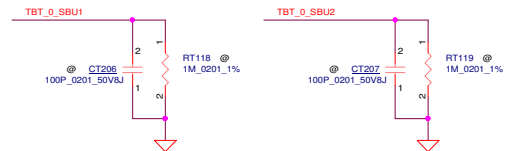
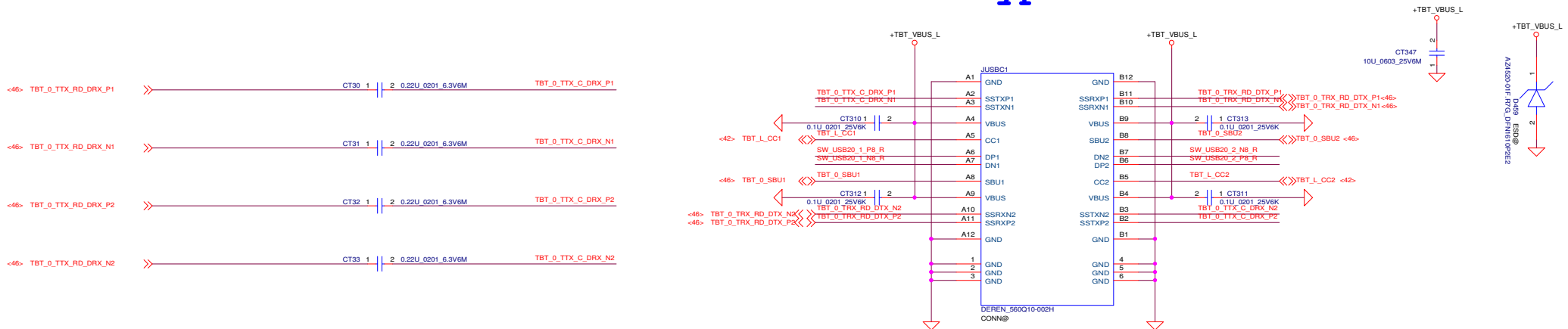
Pin1 : +3V
Pin2 : GND
Pin3 : XRS
Pin4 : SWD_CLK
Pin5 : SWD_DAT

DVT1_29 : update Darwin2.0 block diagram
DVT2_30

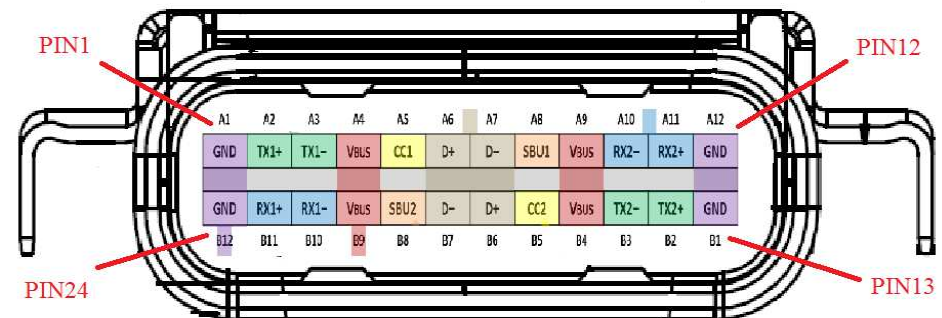
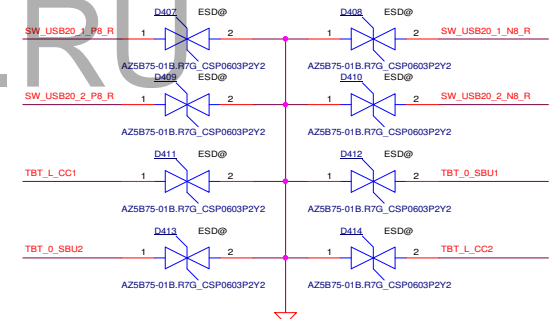


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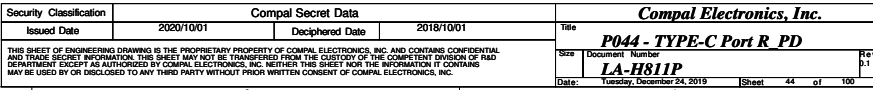
LEFT Type-C Connector



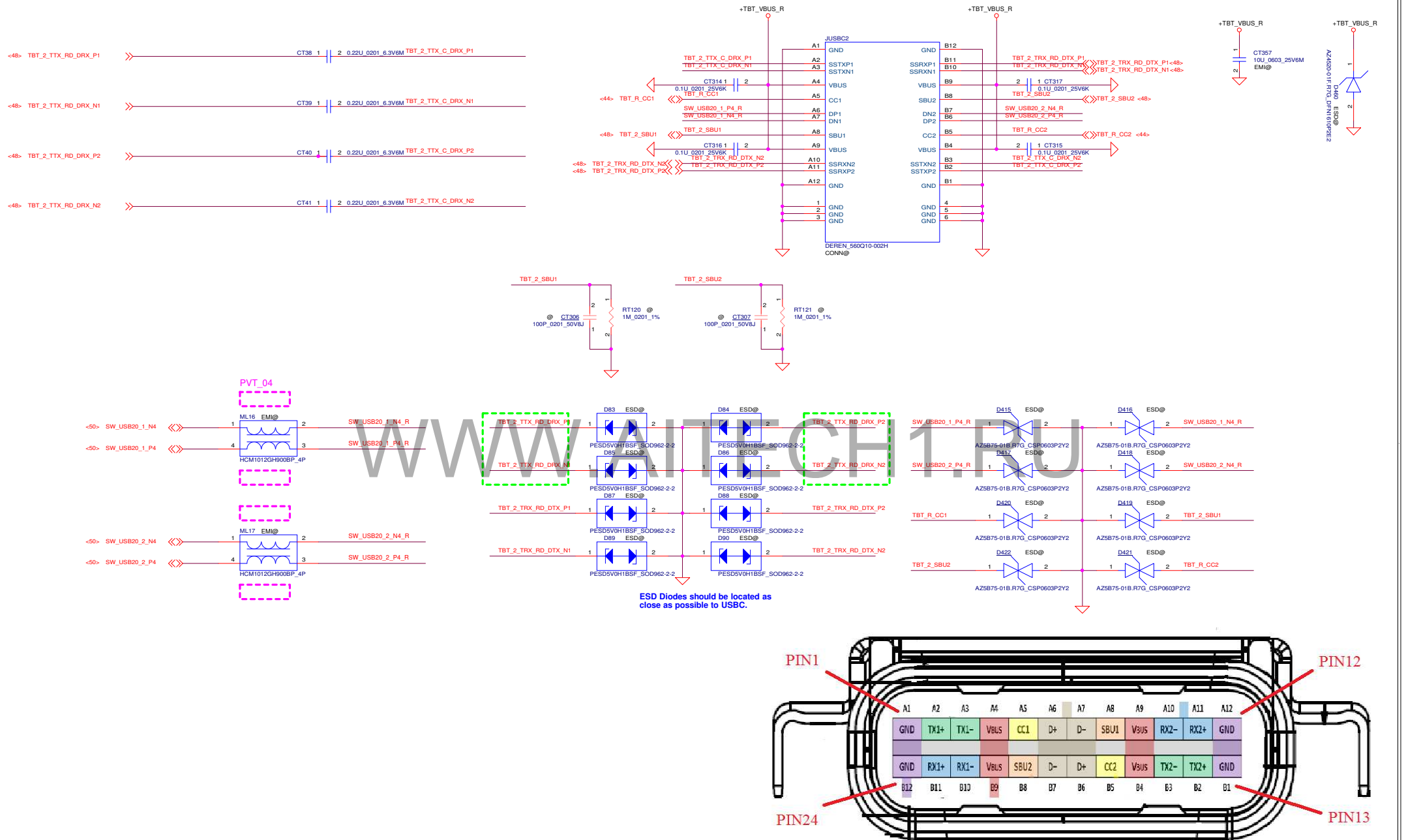
ESD Diodes should be located as close as possible to USBC.



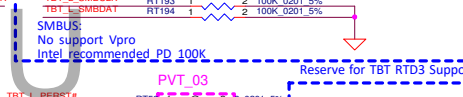
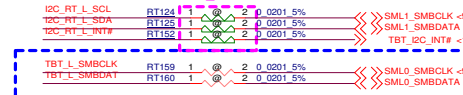
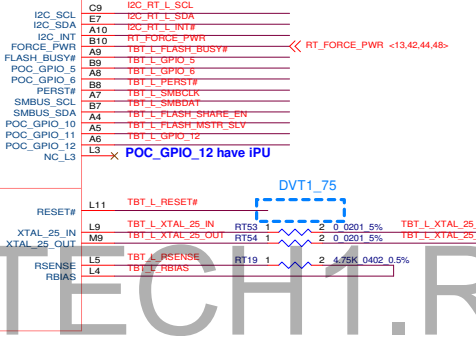
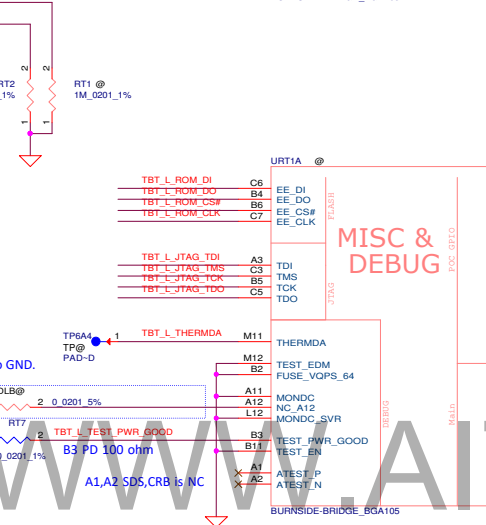
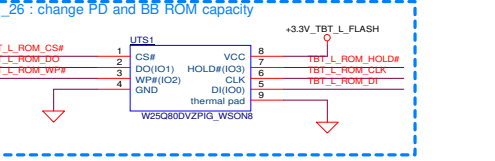
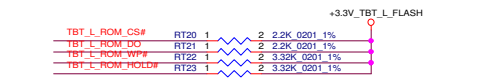
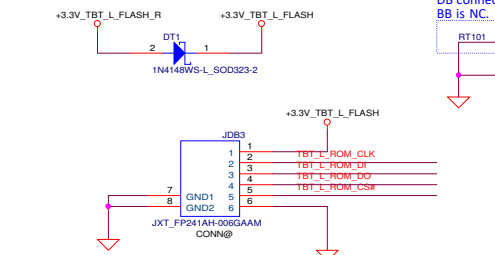
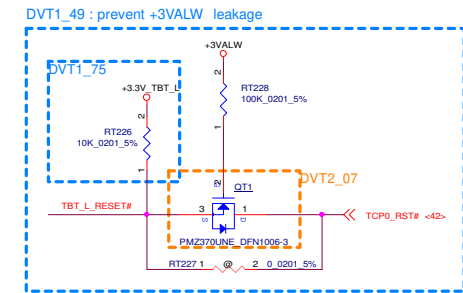
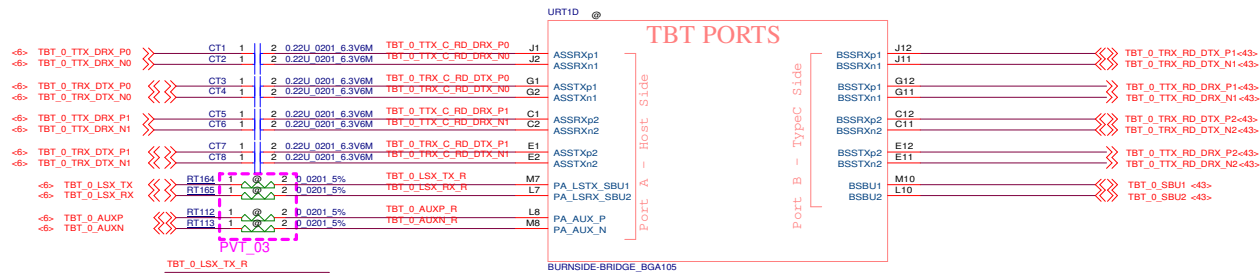
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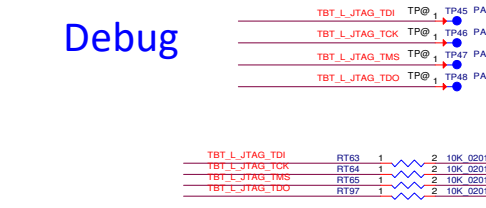
RIGHT Type-C Connector



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Debug



(L11) DG_P1_RST#:
For PD based systems, DG_P1_RST# should be output from PD.
For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR: Connect to PCH for FW update
'0' - by default
'1' - for debug only

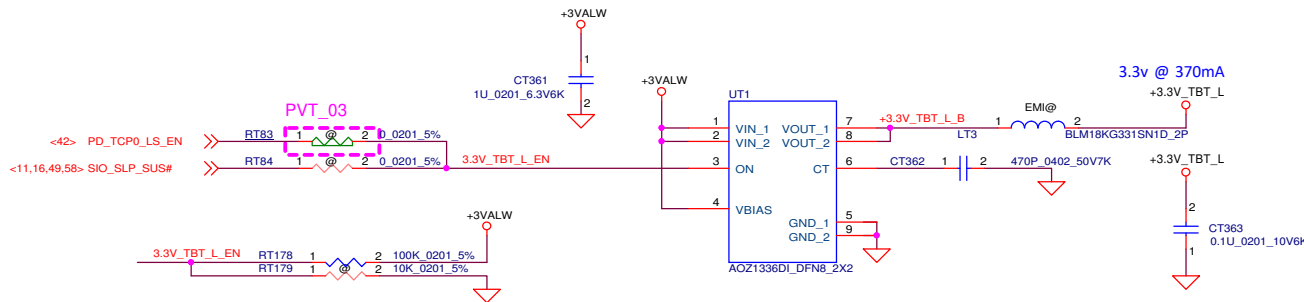
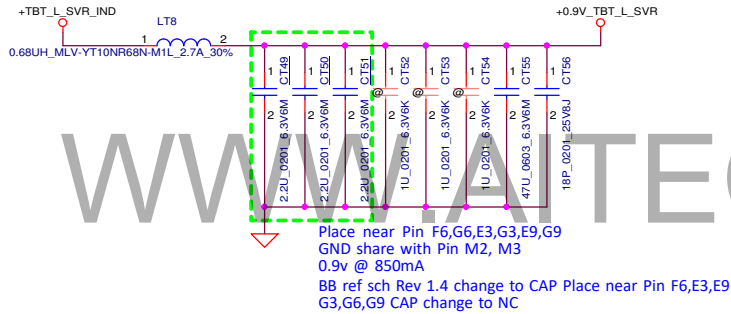
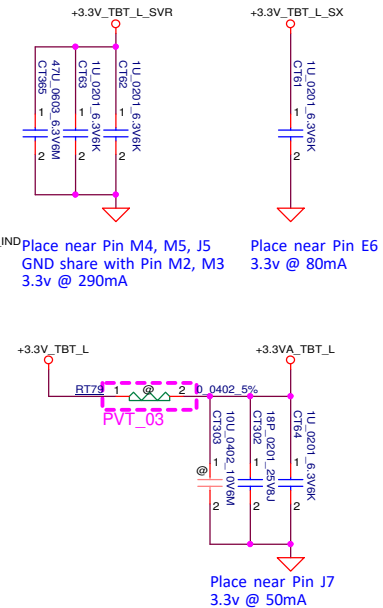
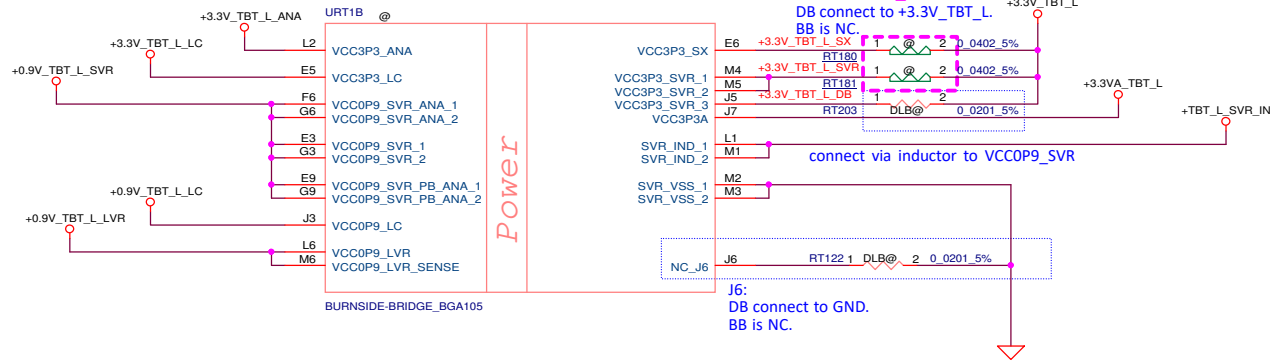
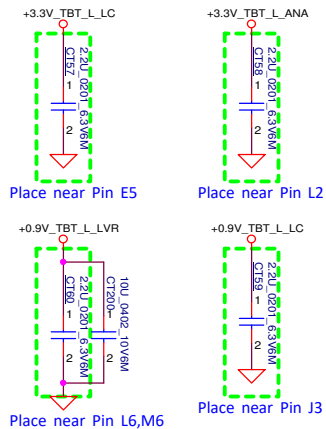
(A9) DG_FLASH_BUSY#: connection to PU

(A4) DG_FLASH_SHARE_EN (IPU):
'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.
'1' - Flash is shared between 2 Re-timers.

(A5) DG_FLASH_MSTR_SLV (IPU):
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:
'0' - Reserved for debug
'1' - Indication to S0 state for Re-timer

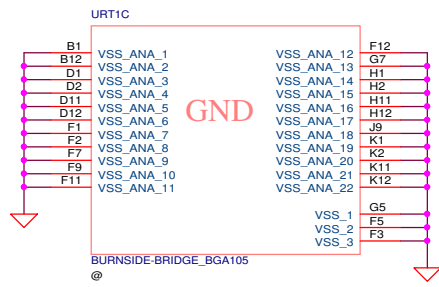
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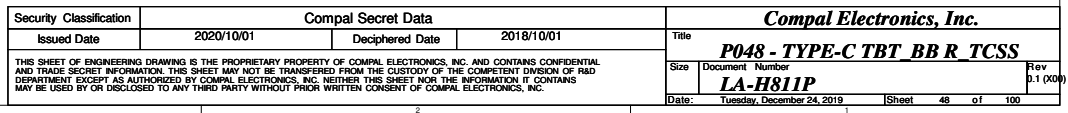
BB ref sch p.6 note
DG_P1_PWR_GATE_EN:

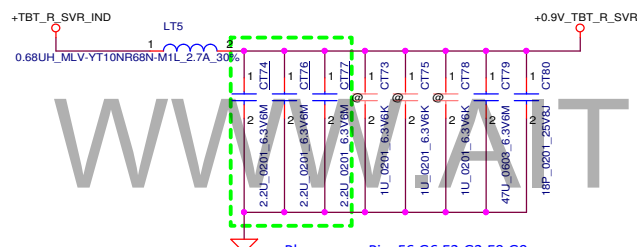
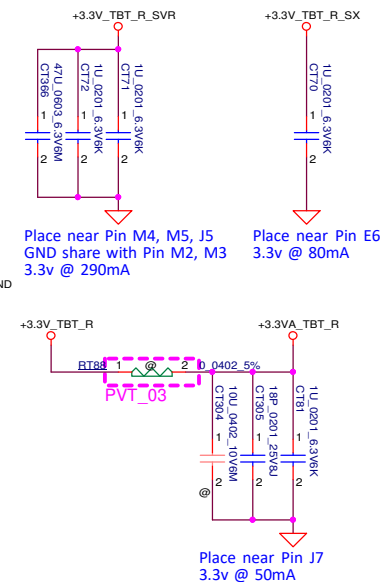
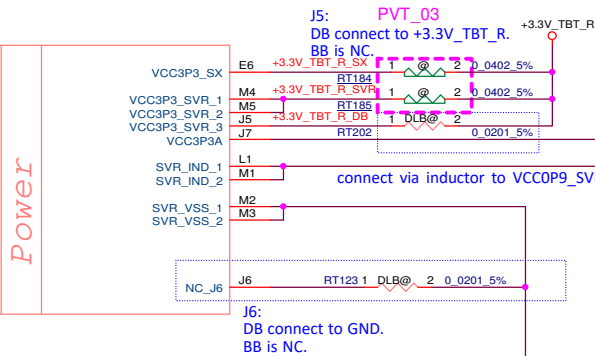
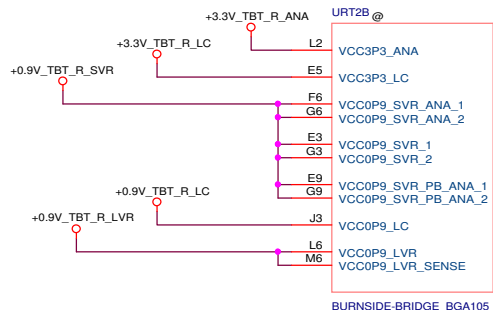
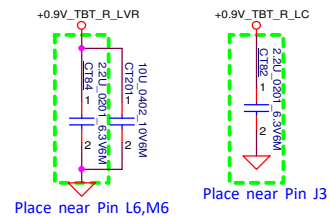
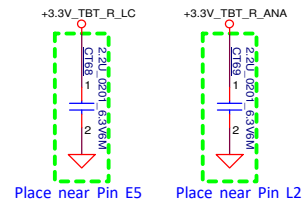
For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.

For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.

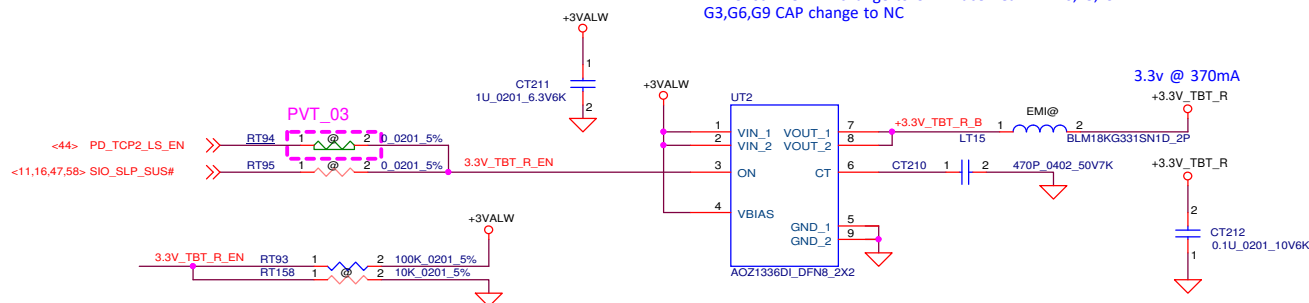


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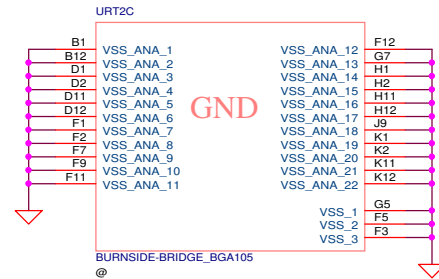




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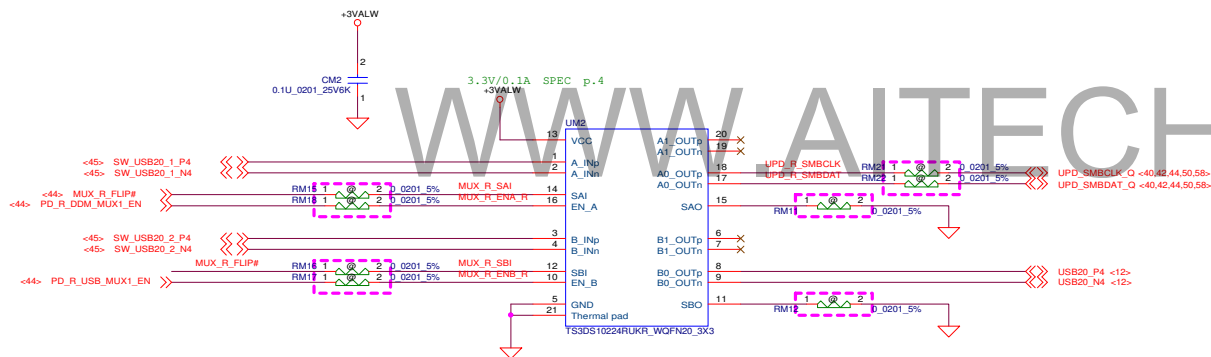


BB ref sch p.6 note
DG_P1_PWR_GATE_EN:
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For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.



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USB2/I2C MUXES_R



Channel	INA	INB
Signal Name	TOP	BOT

					I2C	USB		
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux	Functional Mode
0	1	–	0	–	Hi-Z	TOP	–	USB only on TOP
0	1	–	1	–	Hi-Z	BOT	–	USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint Switch	USB on BOT W/DDM

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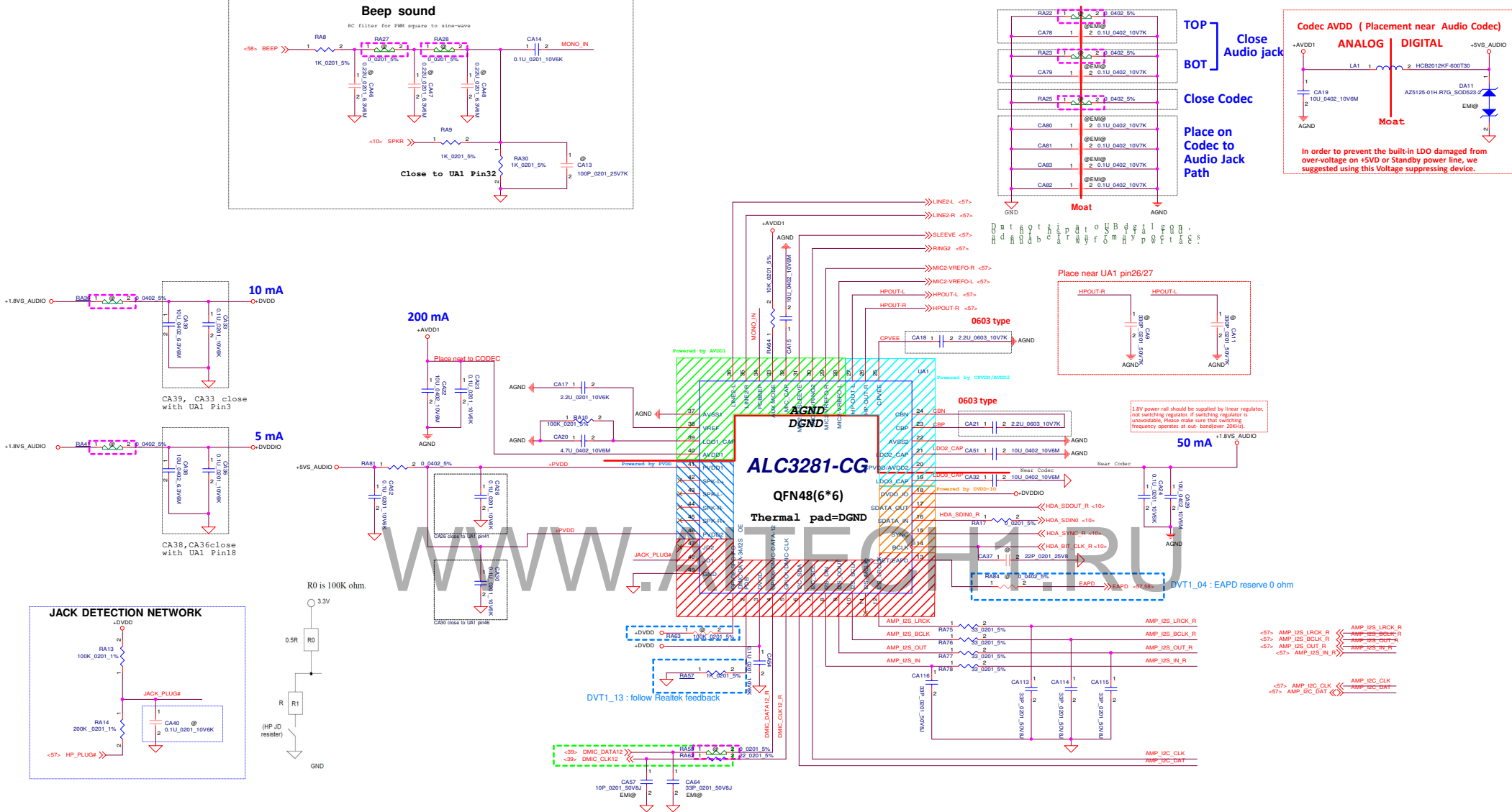
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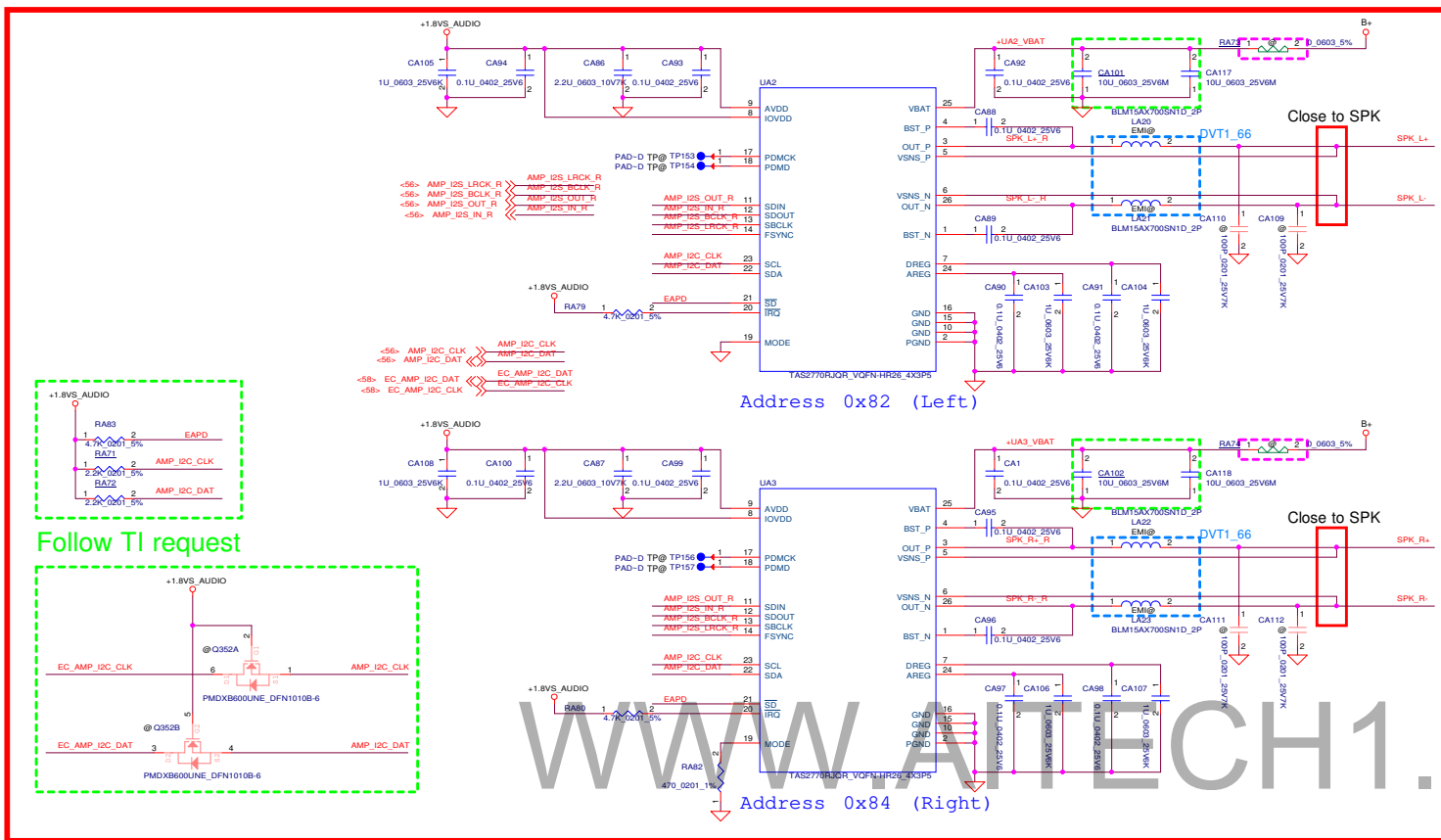
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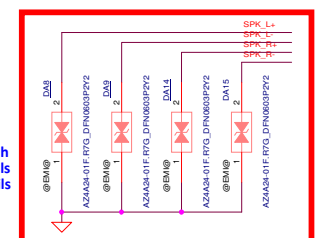
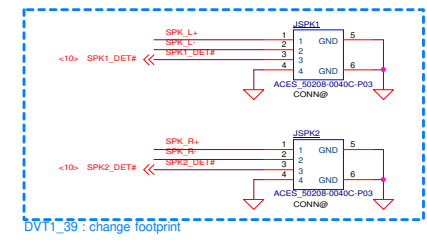
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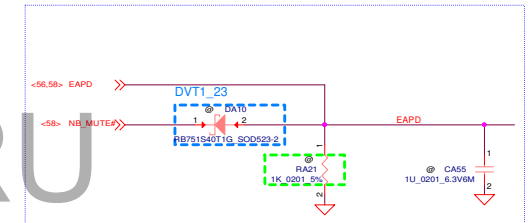


Int. Speaker Conn.



SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

Need up to 15+V, check with EMC



PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

change RA6/RA3 to 5.6 ohm to meet Dell Grade A headphone output power > 25 mW setting

Universal Audio Jack

Universal Audio Jack CONN

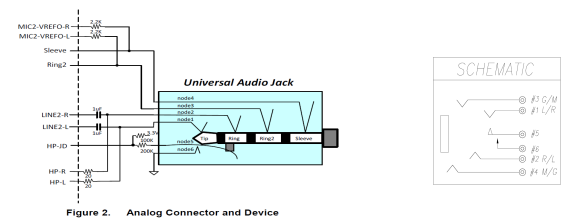
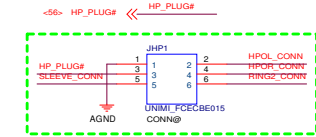
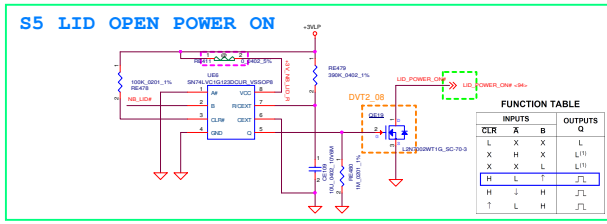
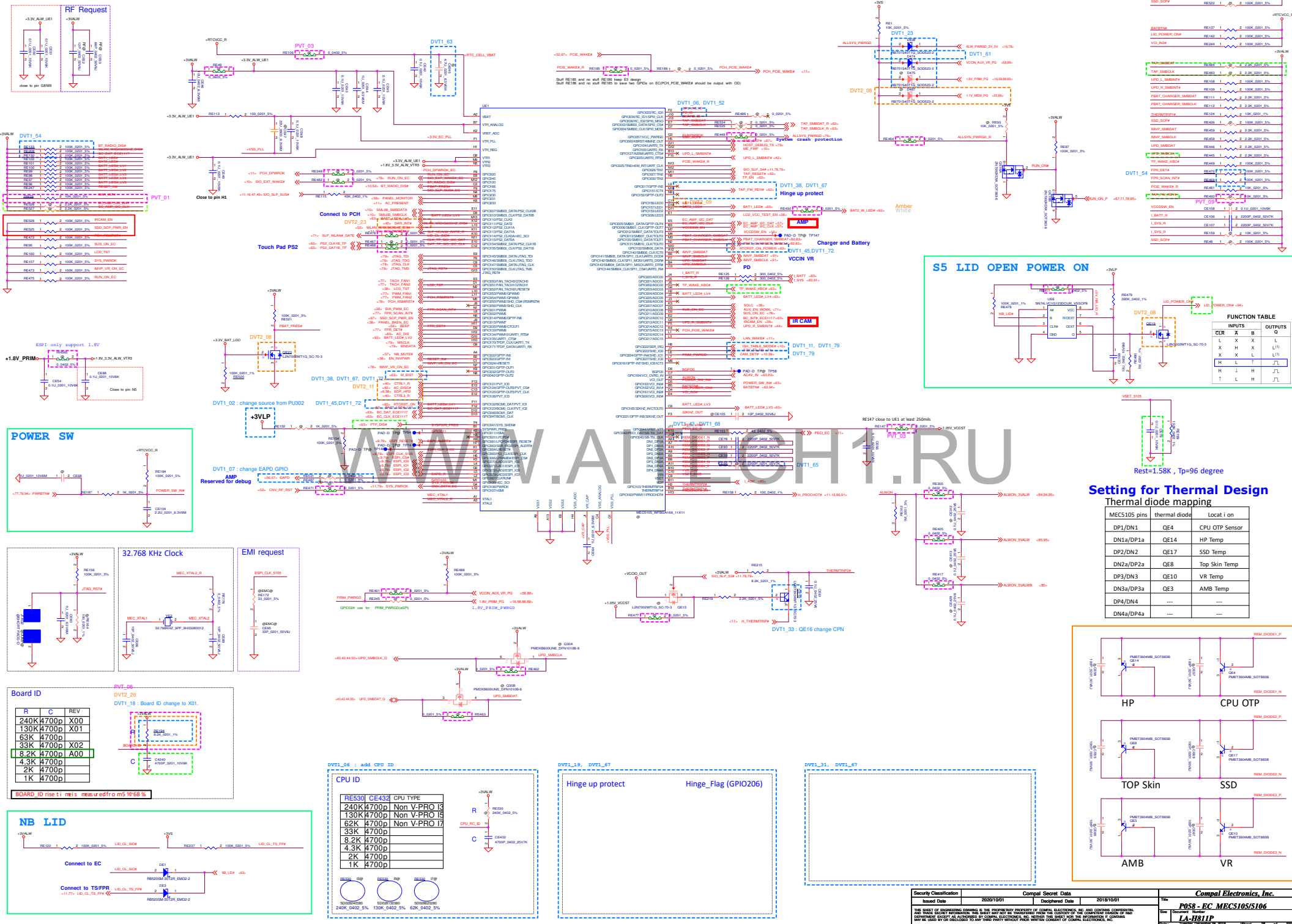


Figure 2. Analog Connector and Device

Contact with PC BEAN



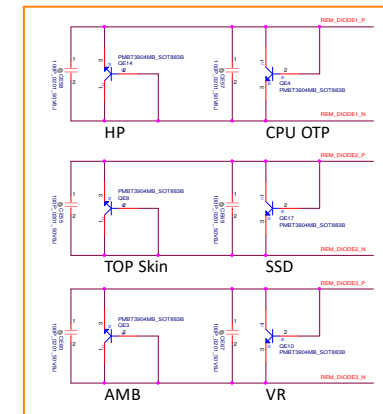
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Setting for Thermal Design

Thermal diode mapping

MECS105 pins	thermal diode	Locat i on
DP1/DN1	QE4	CPU OTP Sensor
DN1a/DP1a	QE14	HP Temp
DP2/DN2	QE17	SSD Temp
DN2a/DP2a	QE10	Top Skin Temp
DP3/DN3	QE13	VR Temp
DN3a/DP3a	QE3	AMB Temp
DP4/DN4	---	---
DN4a/DP4a	---	---

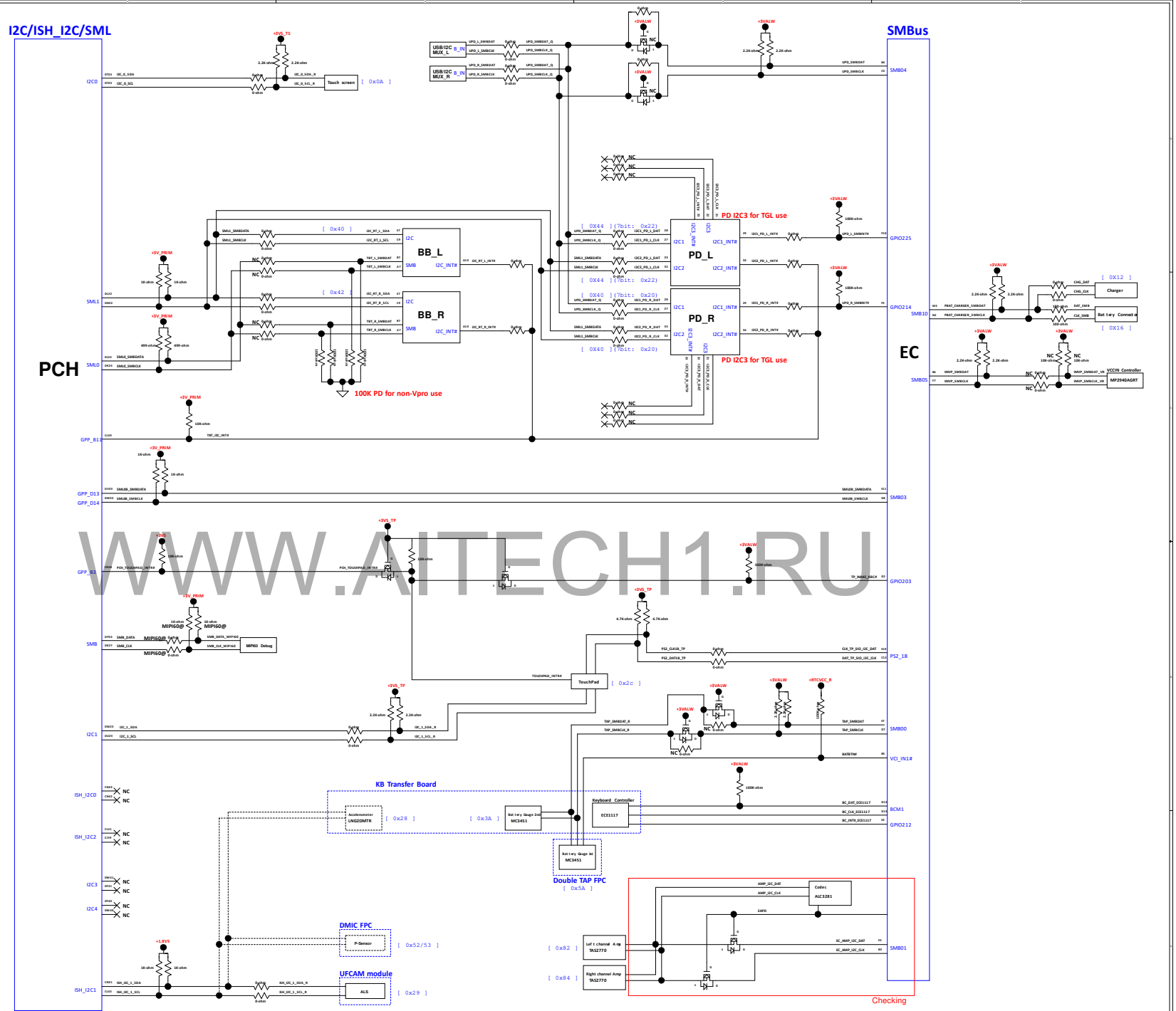


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P061 - SMR22C Block Diagram 1A-SHIP				

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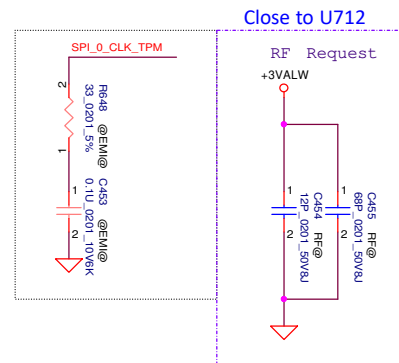
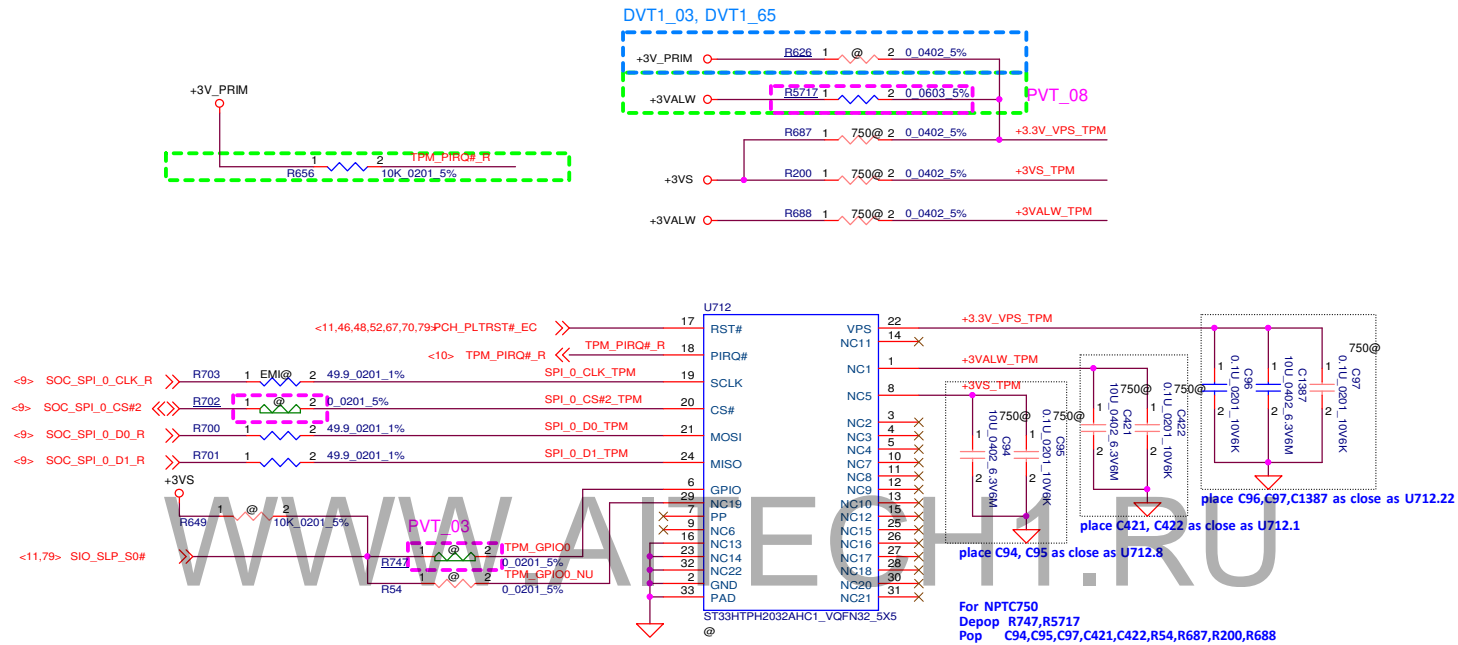
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For ST/Nuvoton TPM



Pin number	1	2	6	8	16	17	18	19	20	21	22	23	24	29
Chip	1	2	6	8	16	17	18	19	20	21	22	23	24	29
ST33	NC	GND	GPIO0	NC	NC	RESET	PIRQ	SCLK	SCS	MOSI	NC	NC	MISO	NC
NPTC750	VDD	NC	NC	RESET	GND						GPIO0			

VSB Standby Power Supply. The VALW power rail 3.3V
VHIO Host Interface Power Supply 3.3V
VPS: Power Supply 3.3V
NPTC750: GPIO0 can be used as a backup option for entering Low-Power mode.

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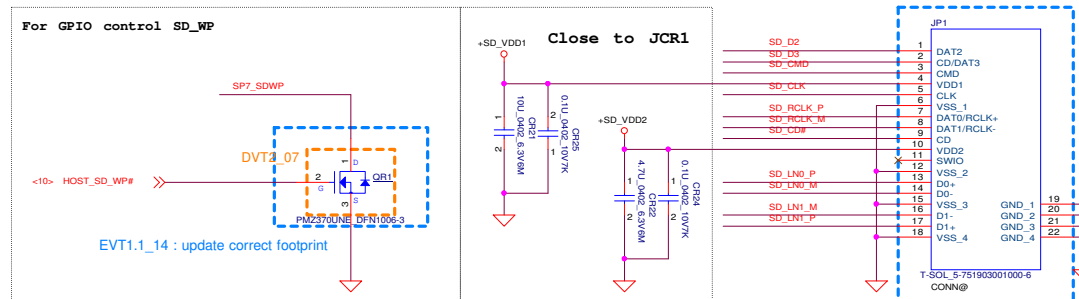
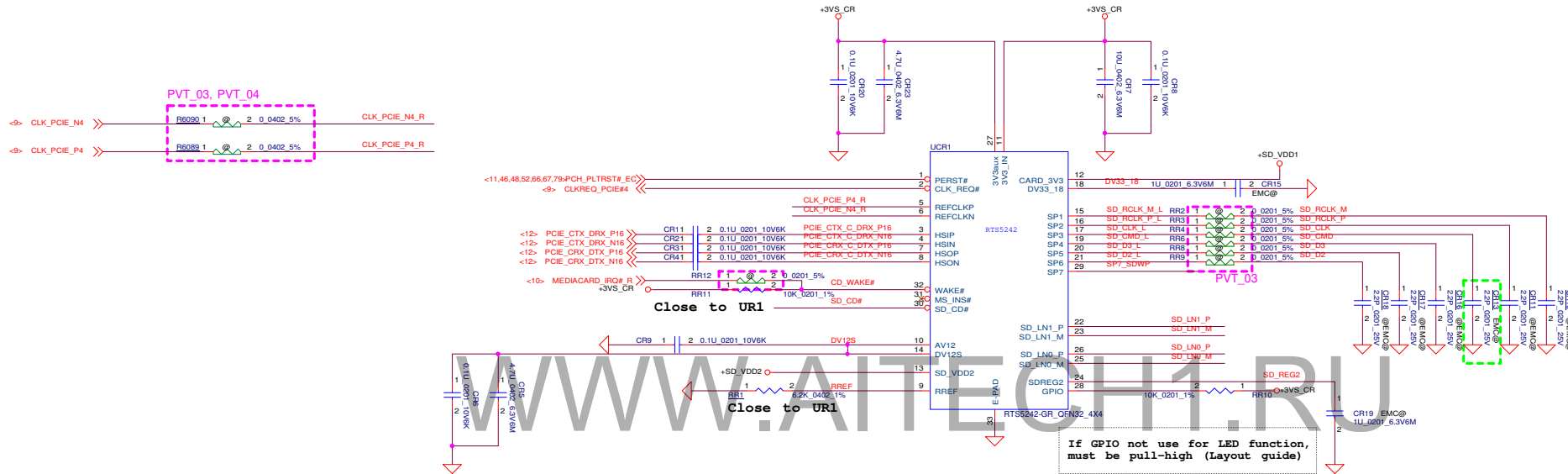
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				Date:	Tuesday, December 24, 2019
				Sheet	69 of 100
				Rev	0.1 (X00)
				LA-H811P	

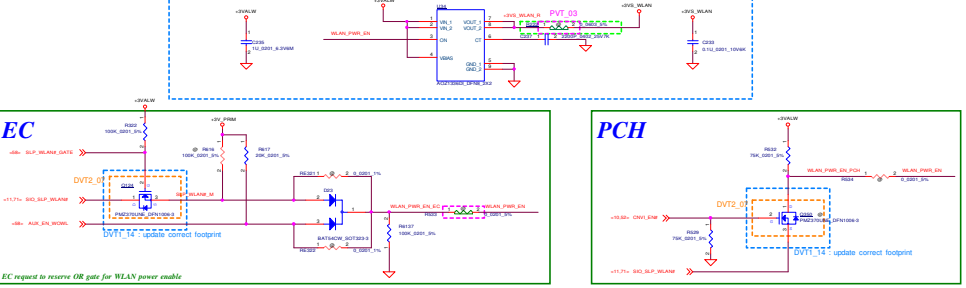
Card Reader

- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.

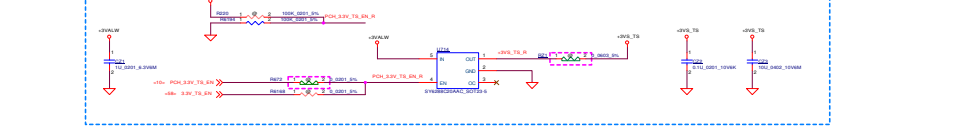


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Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P070 - Card reader uSD RTS5242
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				Date:	Tuesday, December 24, 2019
				Sheet	70 of 100

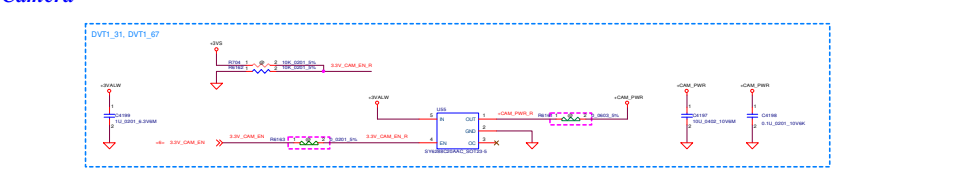
WLAN



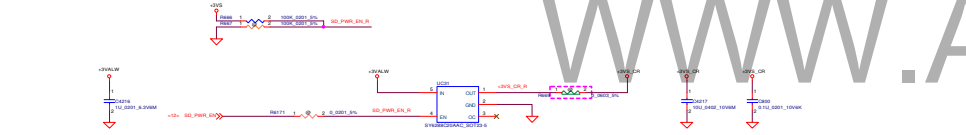
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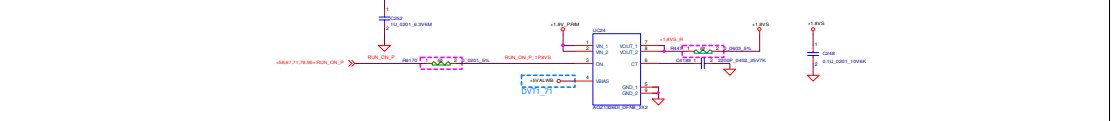
Camera



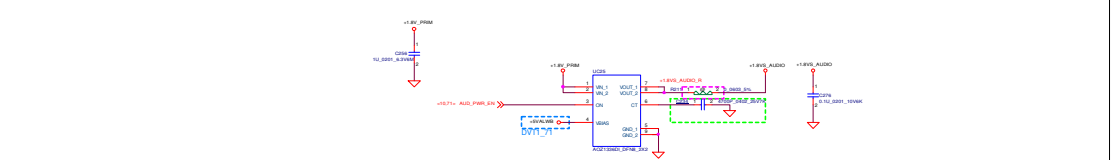
Card Reader



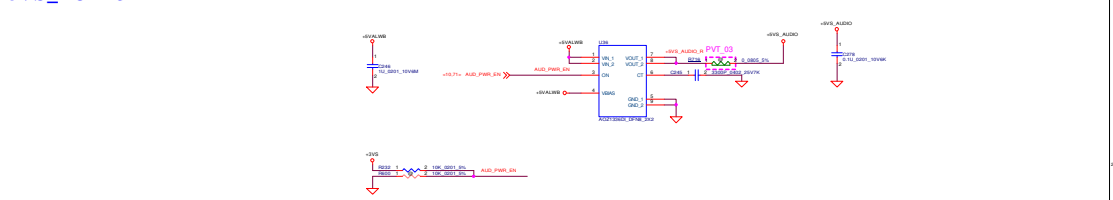
1.8VS



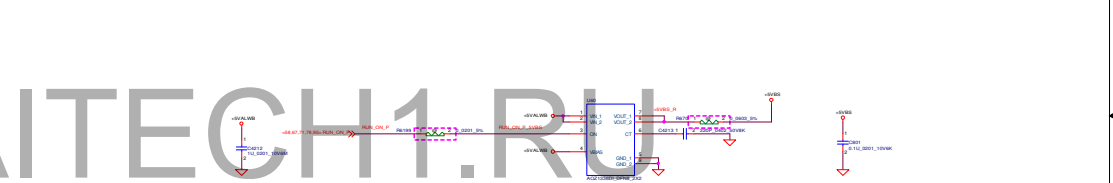
1.8VS_AUDIO



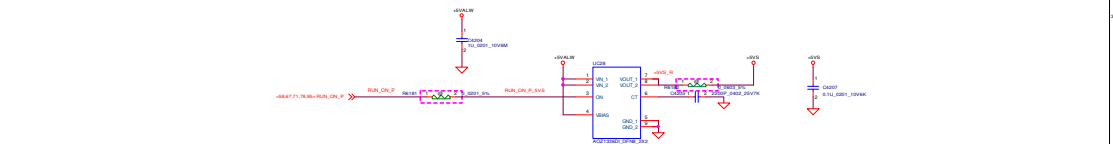
5VS_AUDIO



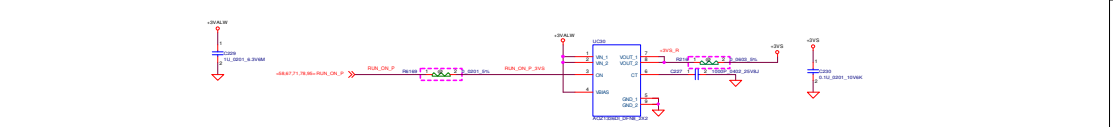
5VBS



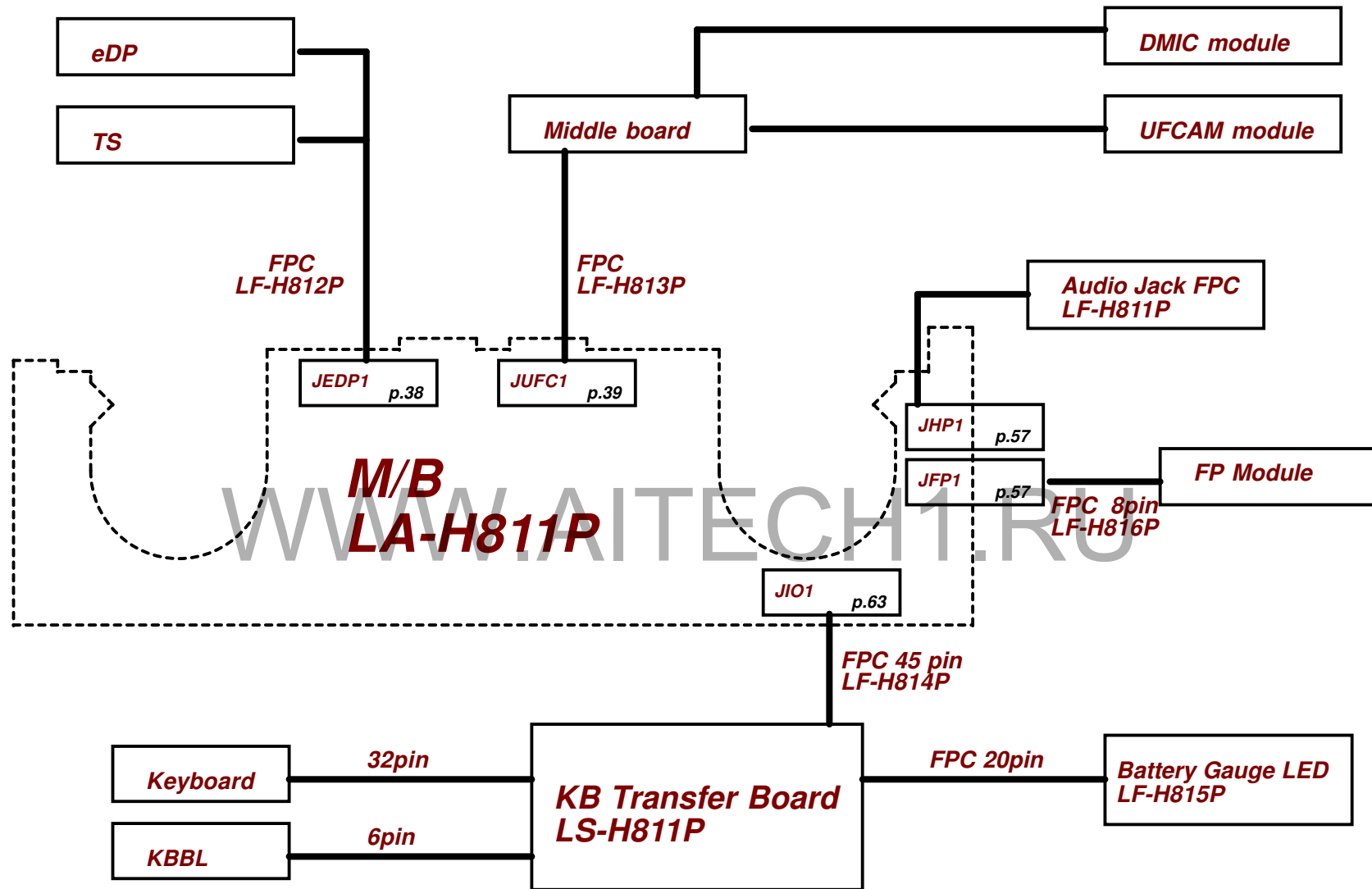
5VS



3VS



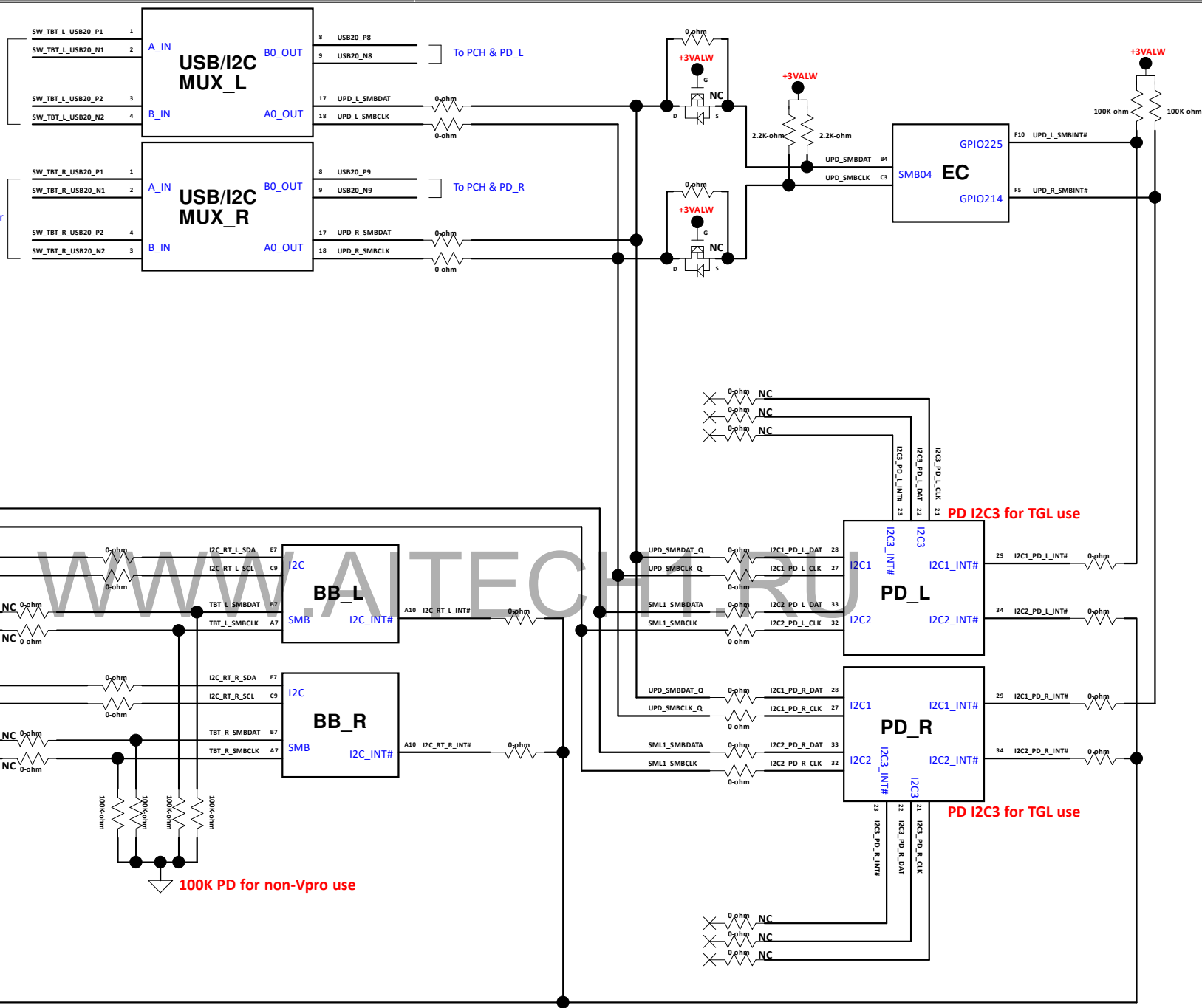
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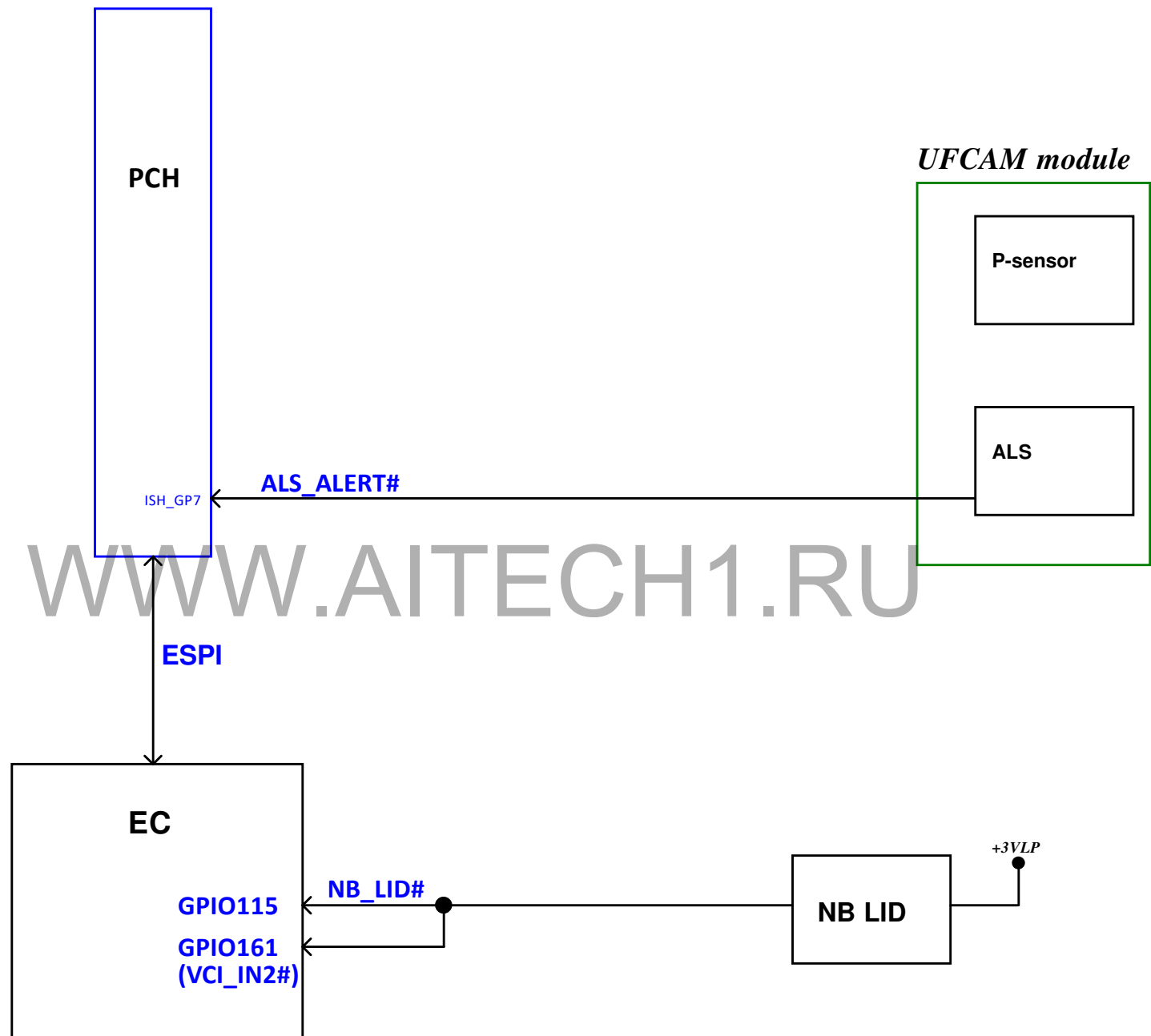


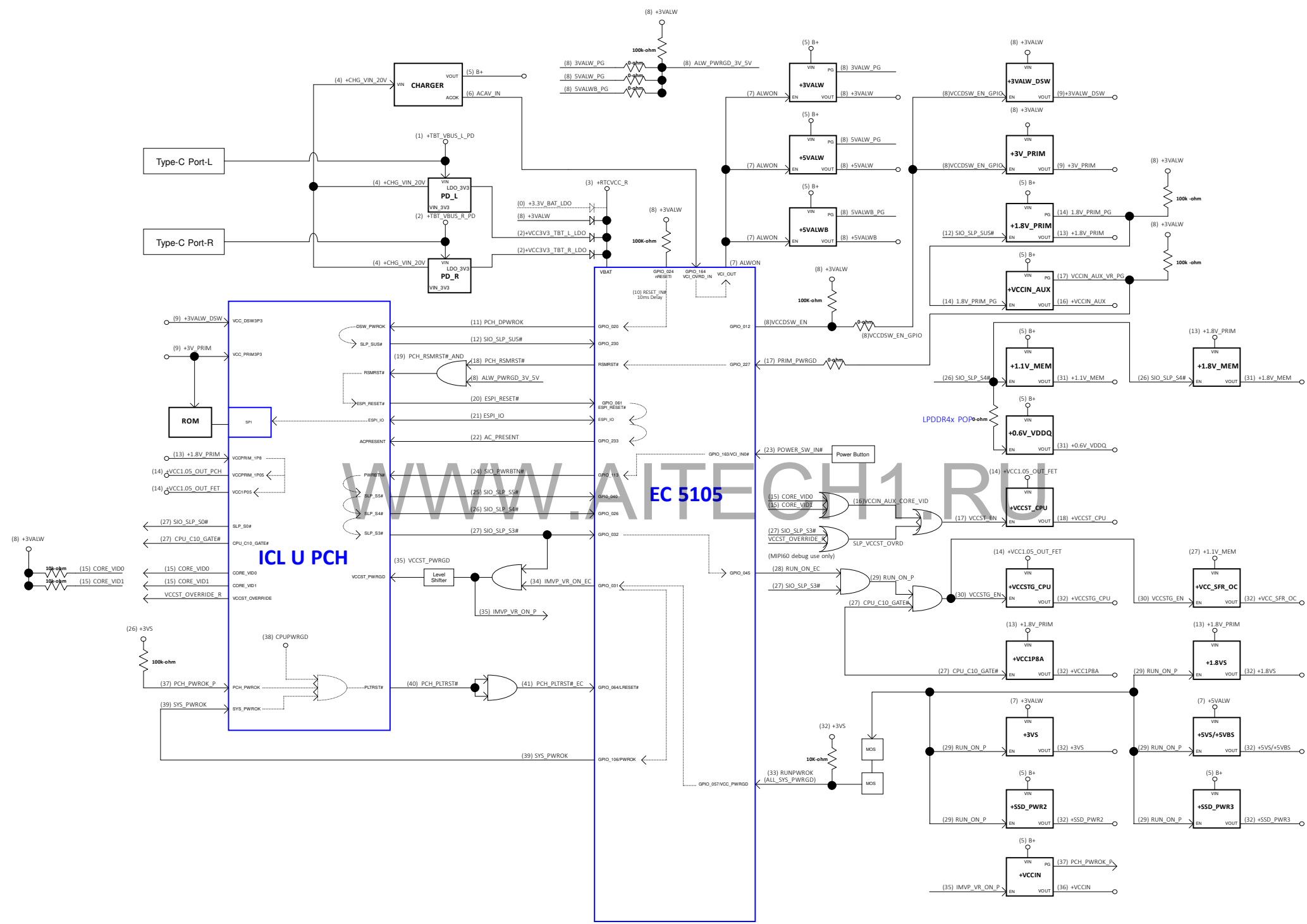
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To LEFT Type-C Connector

To RIGHT Type-C Connector





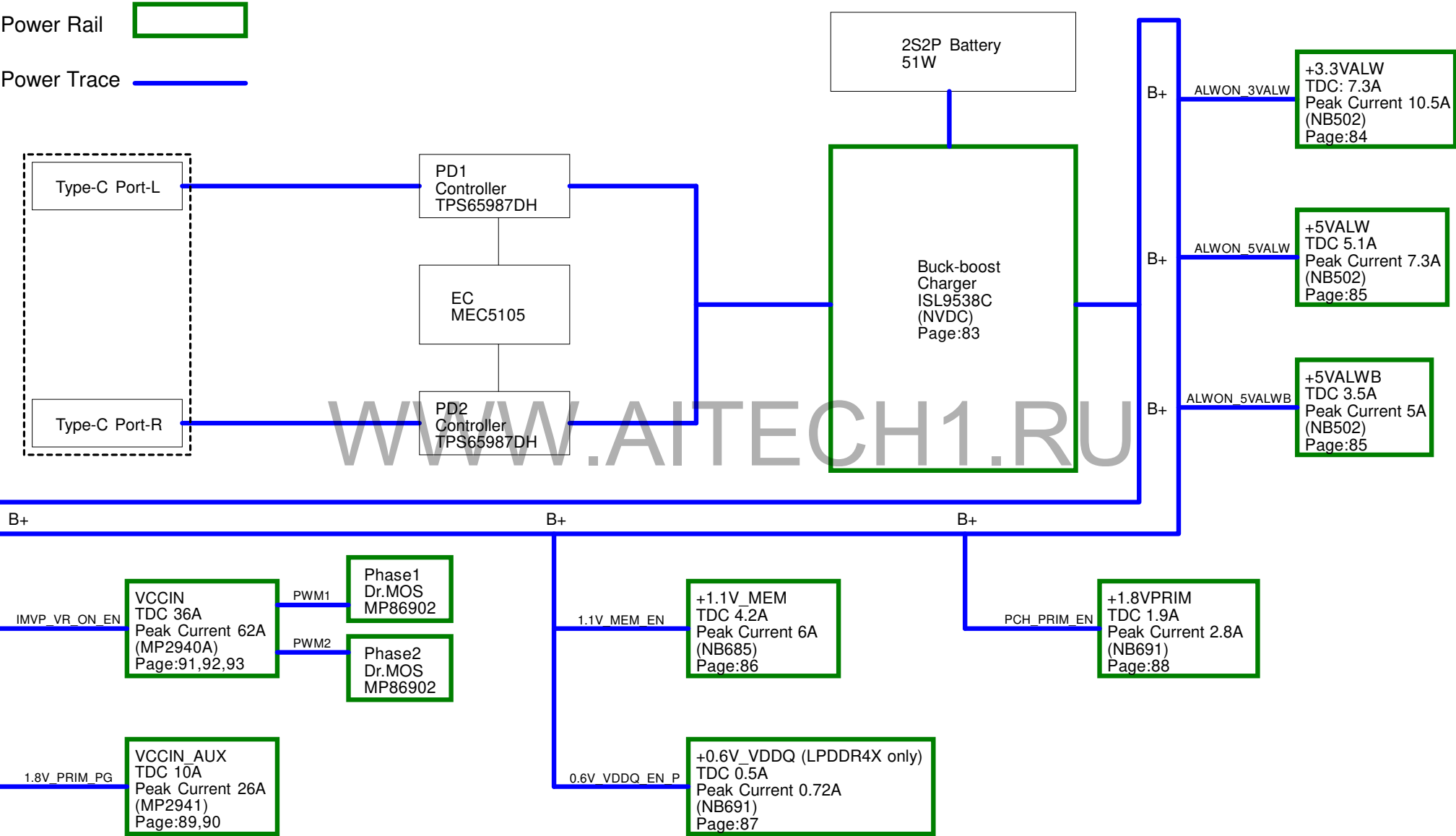


Compal Electronics, Inc.			
Title			
P079 - Debug APS,DEG,eSPI,LED			
Size	Document Number	Rev	
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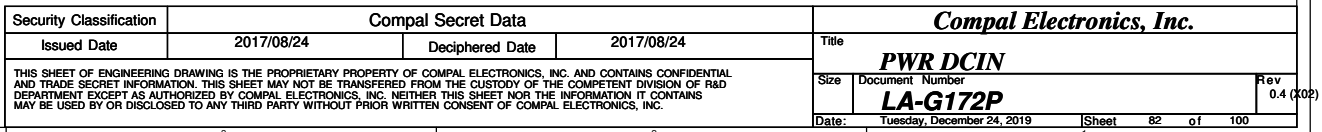
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				LA-H811P	
				Date:	Tuesday, December 24, 2019
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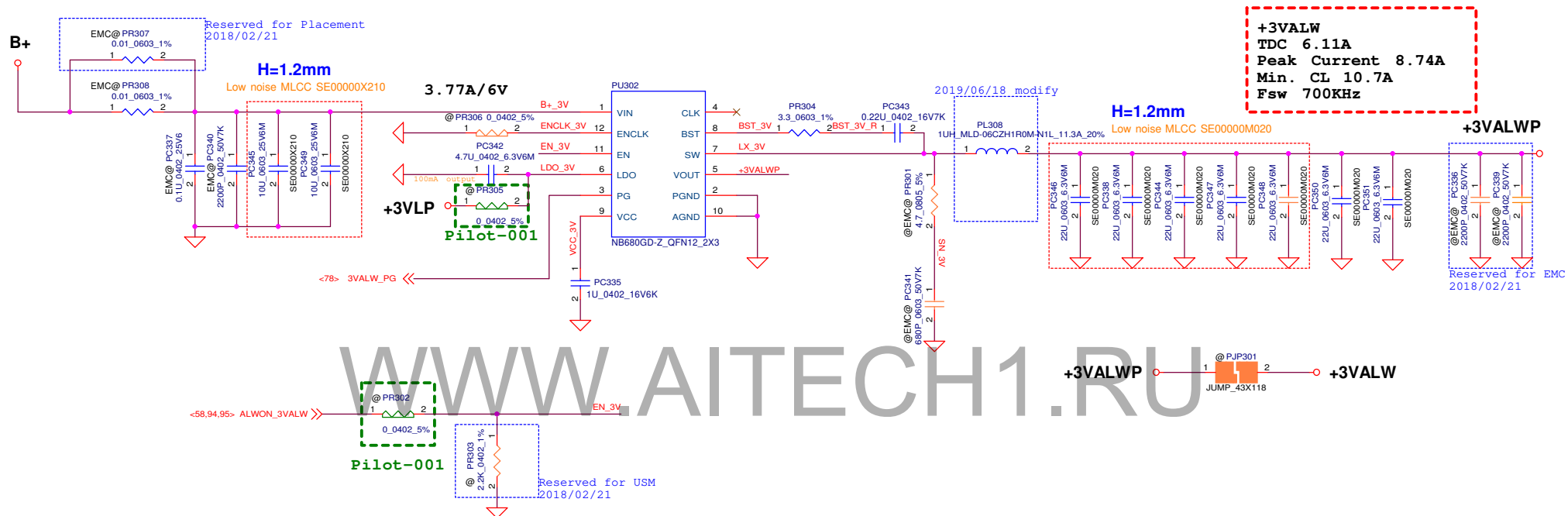
Modena POWER BLOCK DIAGRAM



DCIN(37.1)

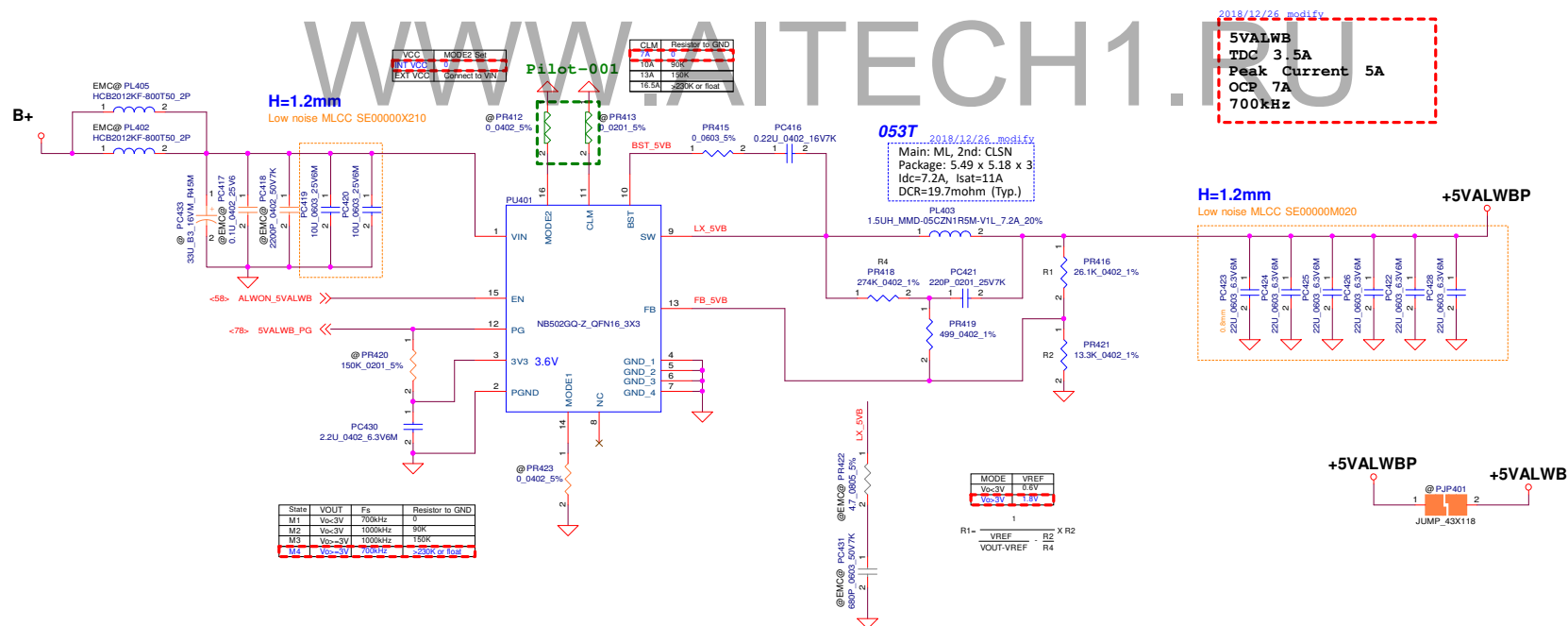
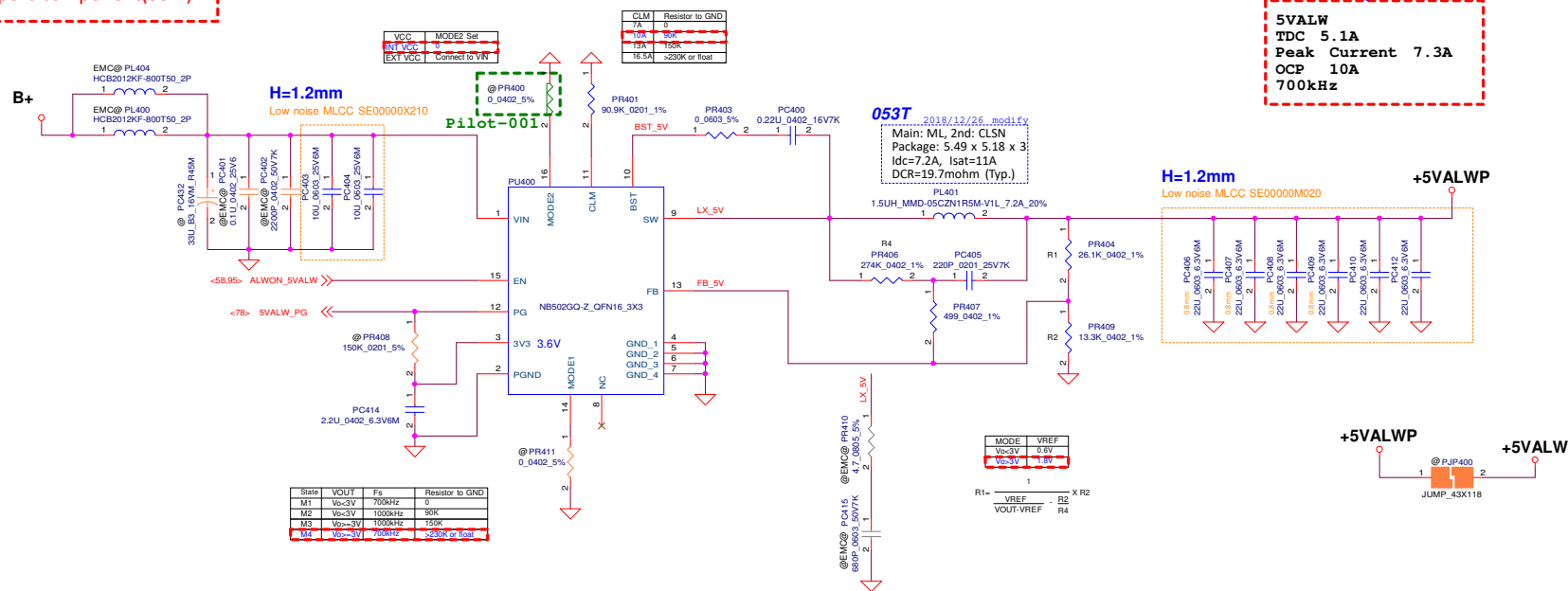


Controller(35.1), Support component(35.2)



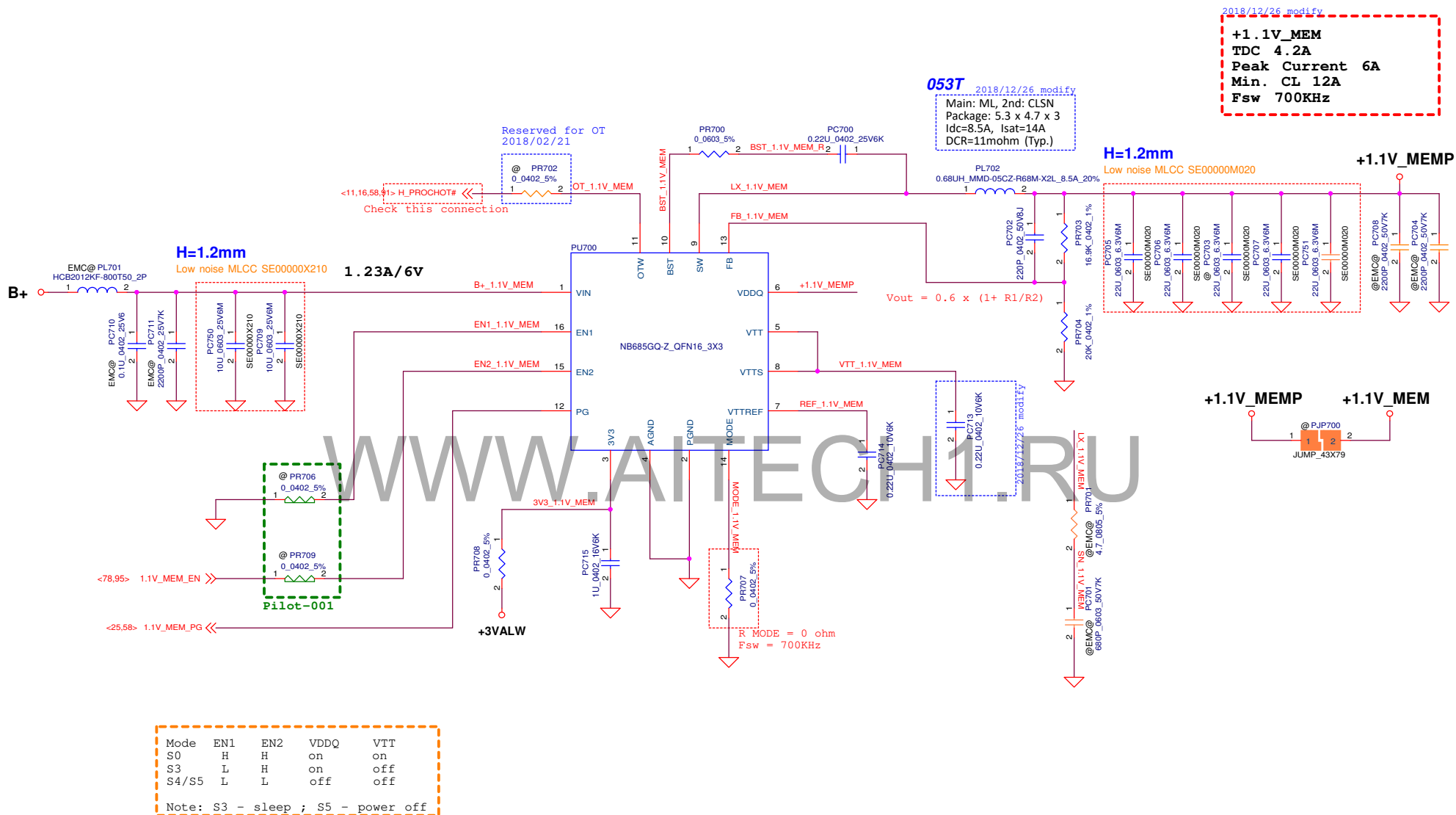
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title PWR +3VALW		
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Controller(35.1), Support component(35.2)



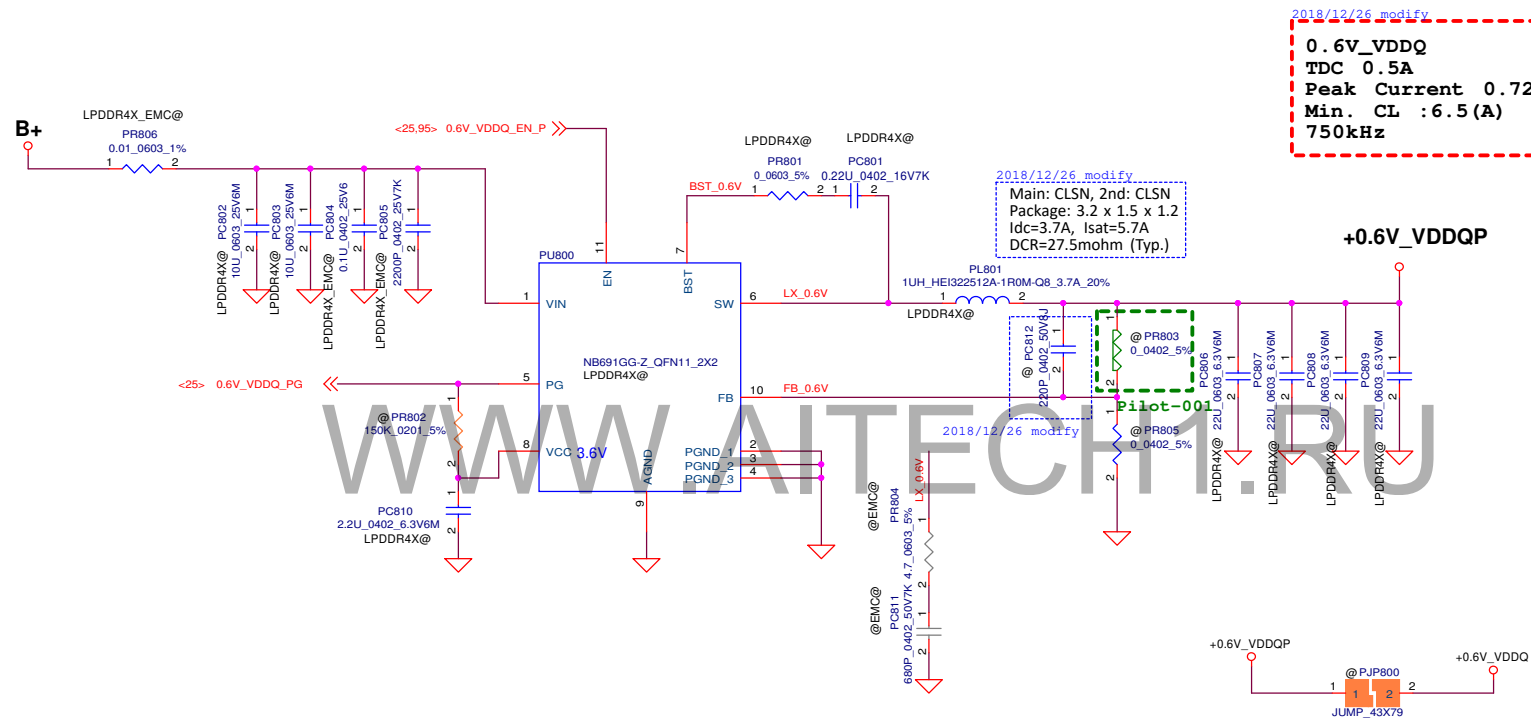
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Issued Date		2017/08/24	Deciphered Date	2017/08/24	Title		
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					Size	Document Number	Rev
					Date:	Tuesday, December 24, 2019	Sheet
					LA-G172P		
					0.4 (2)		

Controller(35.3), Support component(35.4)



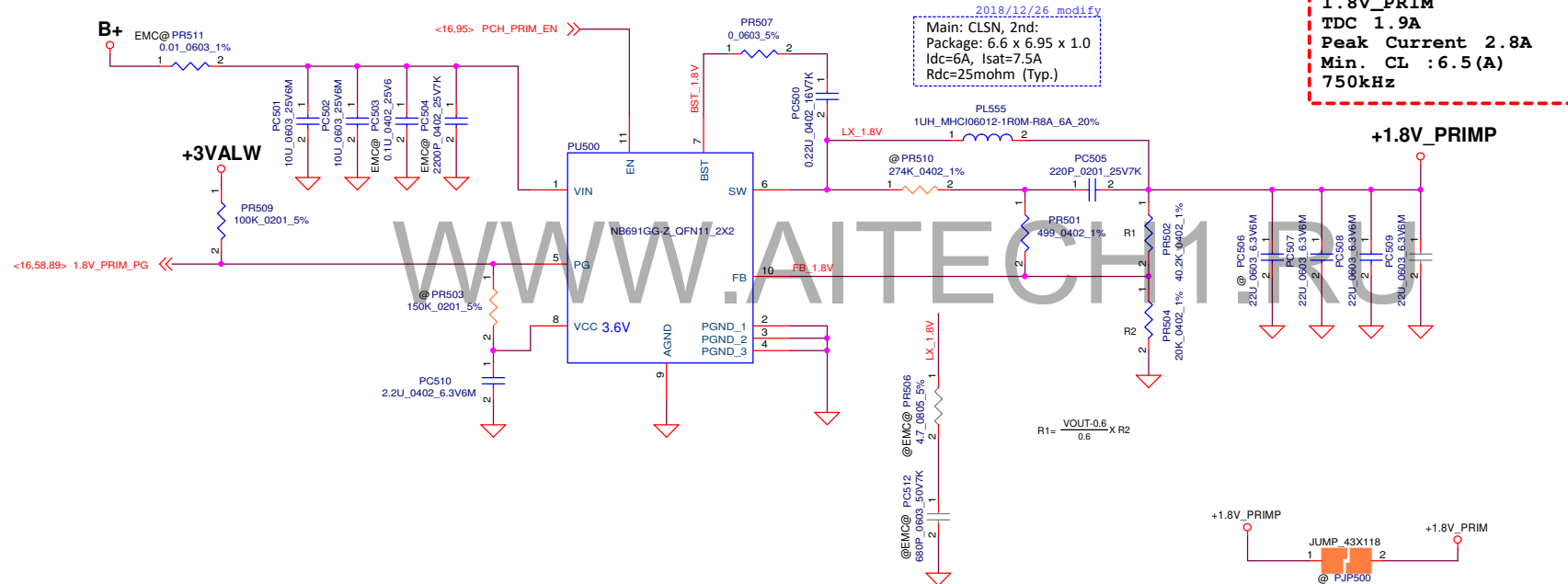
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR +1.1V MEM	
Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	
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Controller(35.3), Support component(35.4)



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Controller(35.13), Support component(35.14)



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				Document Number	0.4 (002)
				LA-G172P Date: Tuesday, December 24, 2019 Sheet 68 of 100	

Controller(36.1), Support component(36.3)

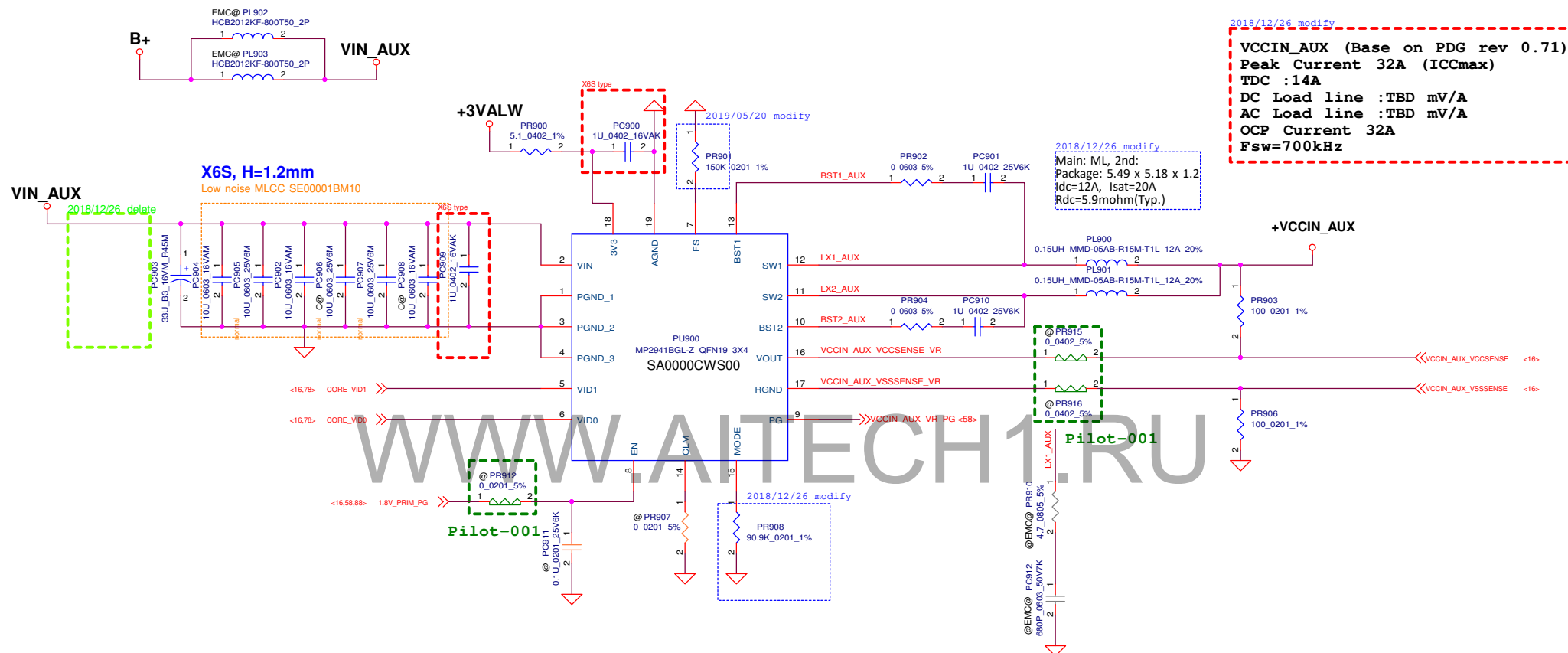


Table---1:VID control Bit logics

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

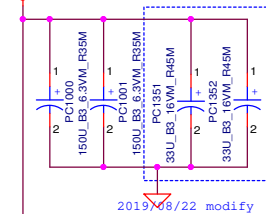
State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs (kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

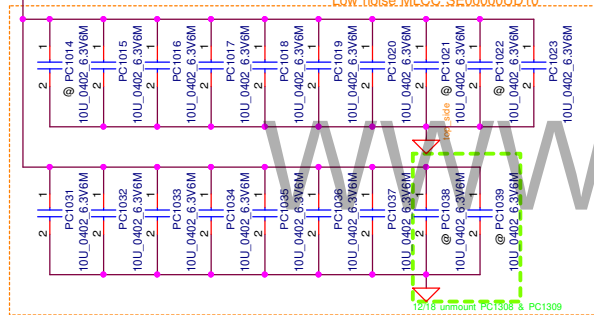
Primary side

+VCCIN_AUX



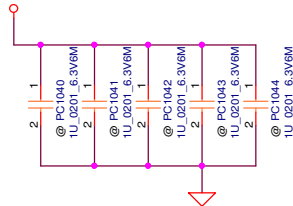
H=0.8mm

Low noise MLCC SE00000UD10

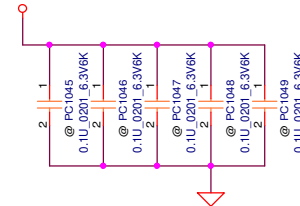


Backside

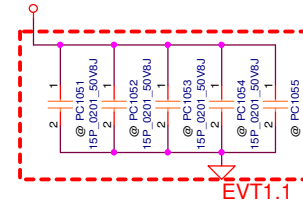
+VCCIN_AUX



+VCCIN_AUX



+VCCIN_AUX



150U_B3 * 4 (POP*2, NC*2)
 10U_0402 * 19 (POP*14, NC*5)
 22U_0603 * 10 (POP*1, NC*9)
 47U_0603 * 7 (POP*1, NC*6)
 1U_0201 * 5 (NC*5)
 0.1U_0201 * 5 (NC*5)

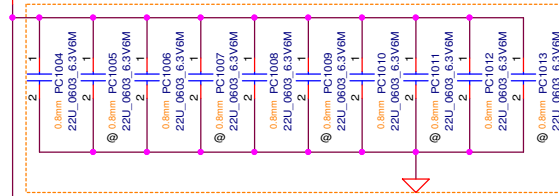
PDG ver 1.1 Primary side:

2x 330uF 7343
 3x 22uF 0603
 12x 10uF 0402
 1x 47uF 0805

+VCCIN_AUX

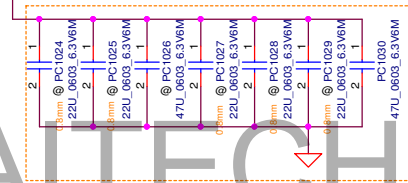
H=1.2mm

Low noise MLCC SE00000M020



H=1.2mm

Low noise MLCC SE000015510

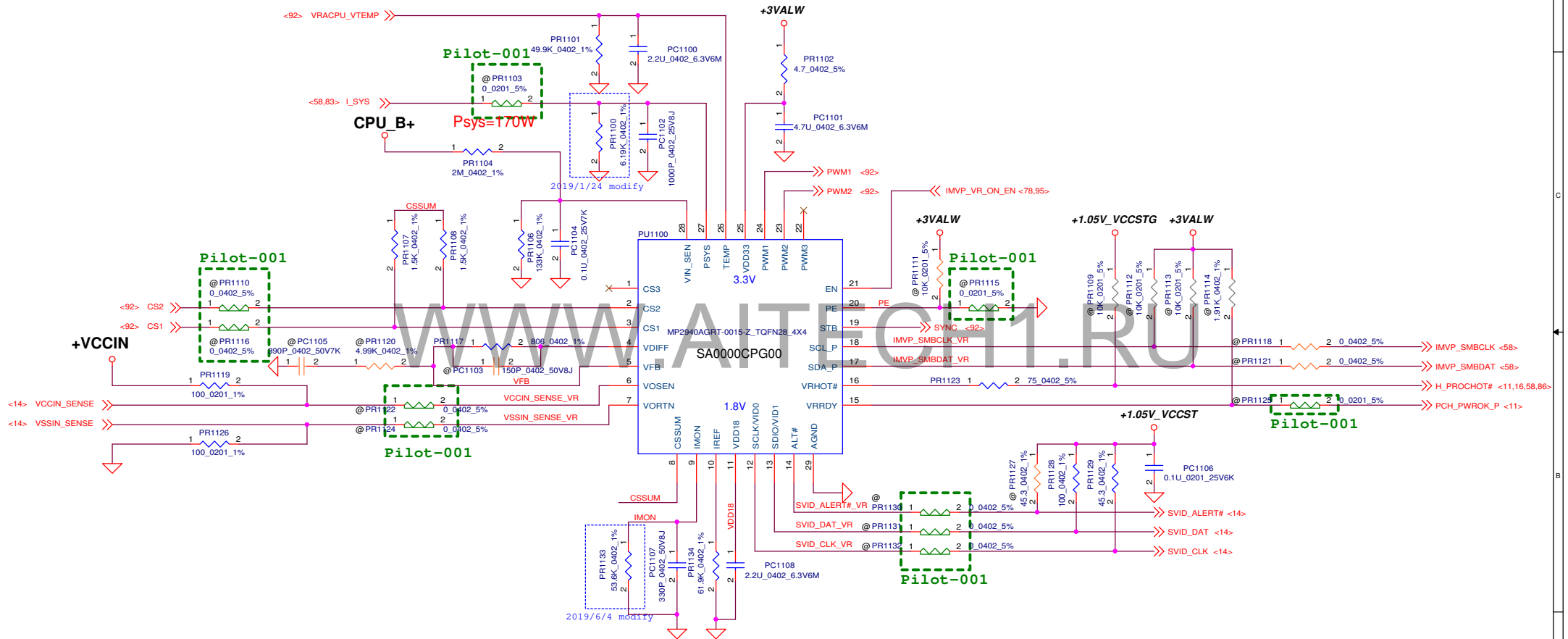


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Controller(36.1), Support component(36.3)

VCCIN (Base on PDG rev 0.71)
Peak Current 54A (ICCmax)
TDC :25A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz

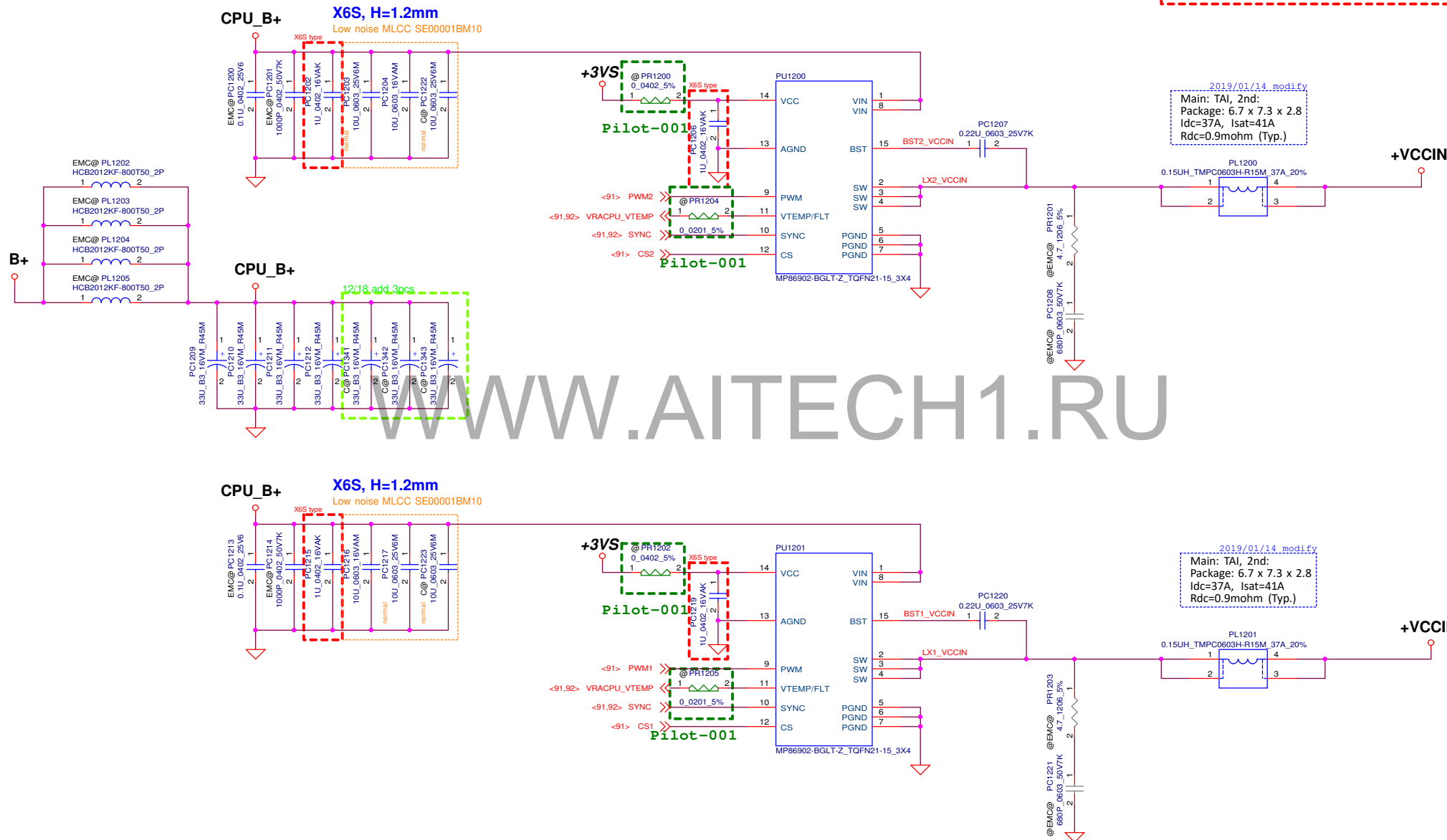


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				Size	Document Number
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Support component(36.2),(36.3)

2018/12/26 modify

VCCIN (Base on PDG rev 0.71)
Peak Current 62A (ICCmax)
PL2 TDC :36A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz

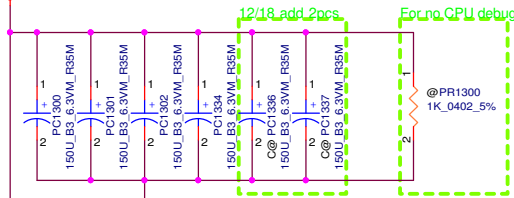


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Size		Document Number		Rev	
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Support component(36.4)

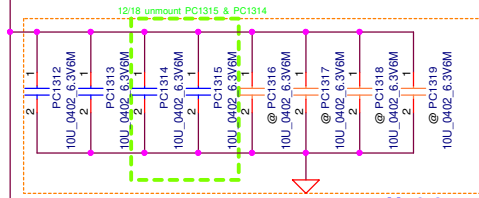
Primary side

+VCCIN

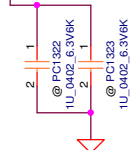


12/18 add 2pcs

For no CPU debug

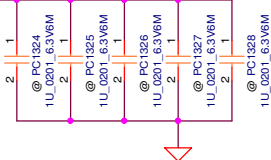


H=0.8mm
Low noise MLCC SE00000UD10

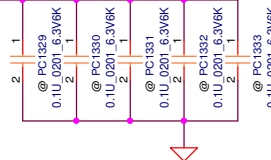


Backside

+VCCIN



+VCCIN



150U_B3 * 4 (pop*2, NC*2)
10U_0402 * 8 (pop*4, NC*4)
22U_0603 * 8 (pop*7, NC*1)
47U_0603 * 2 (NC*2)
1U0402 * 2
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)

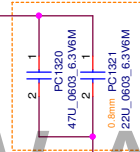
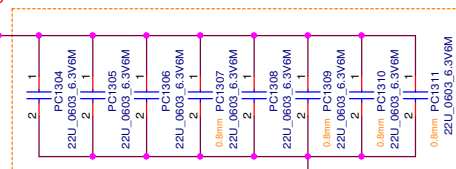
PDG ver 1.1 Primary side:

2x 1uF 0402
4x 10uF 0402
8x 22uF 0603
1x 47uF 0805
2x 330uF 7343

+VCCIN

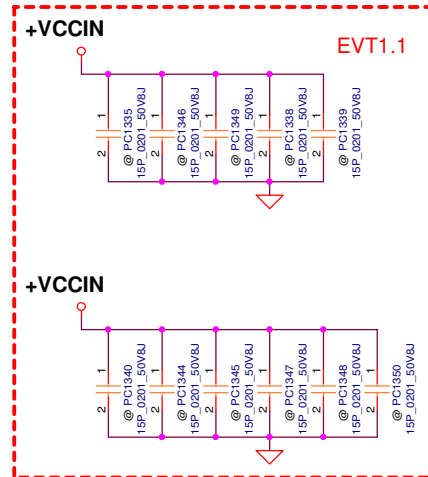
H=1.2mm

Low noise MLCC SE00000M020



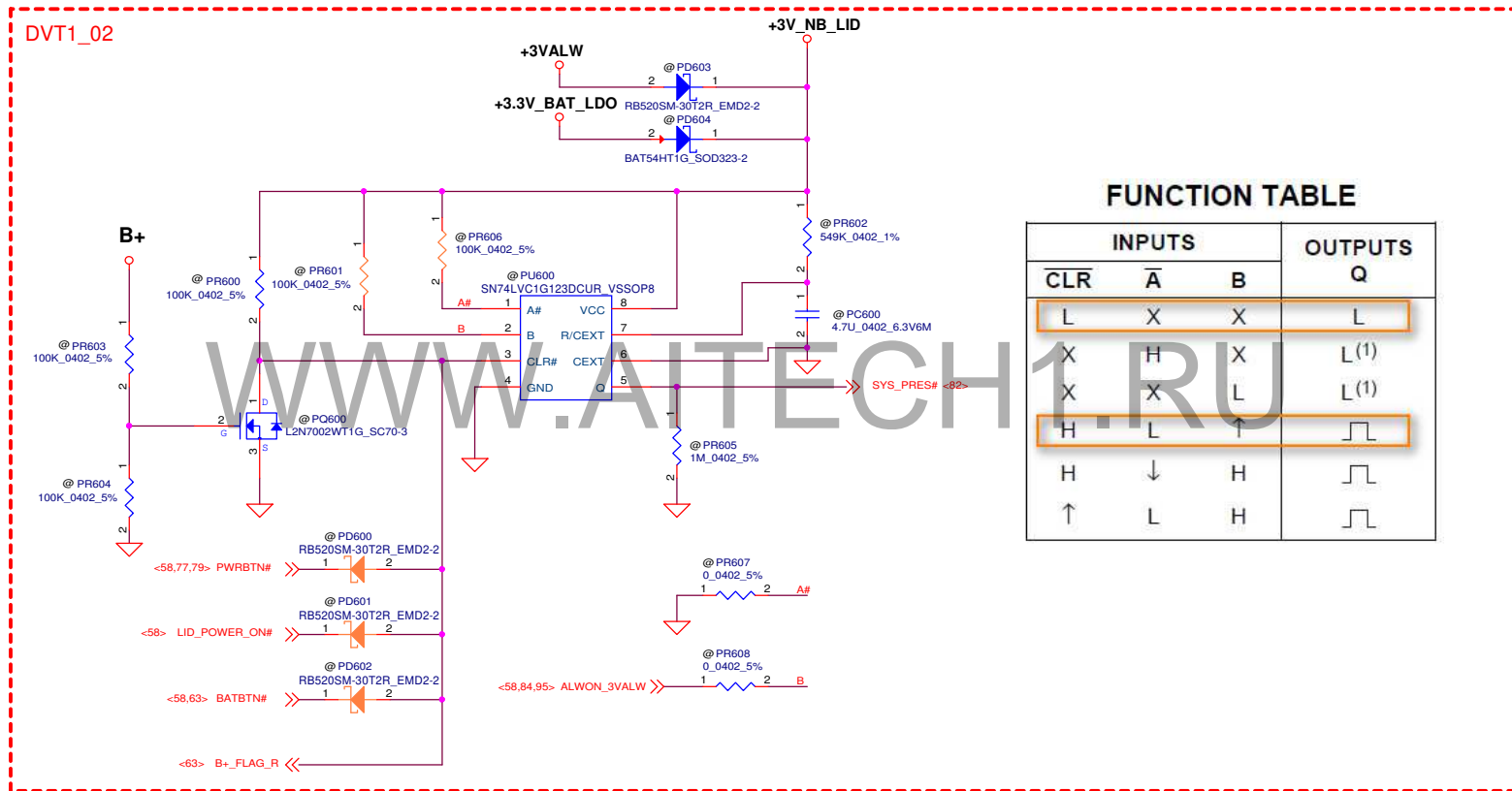
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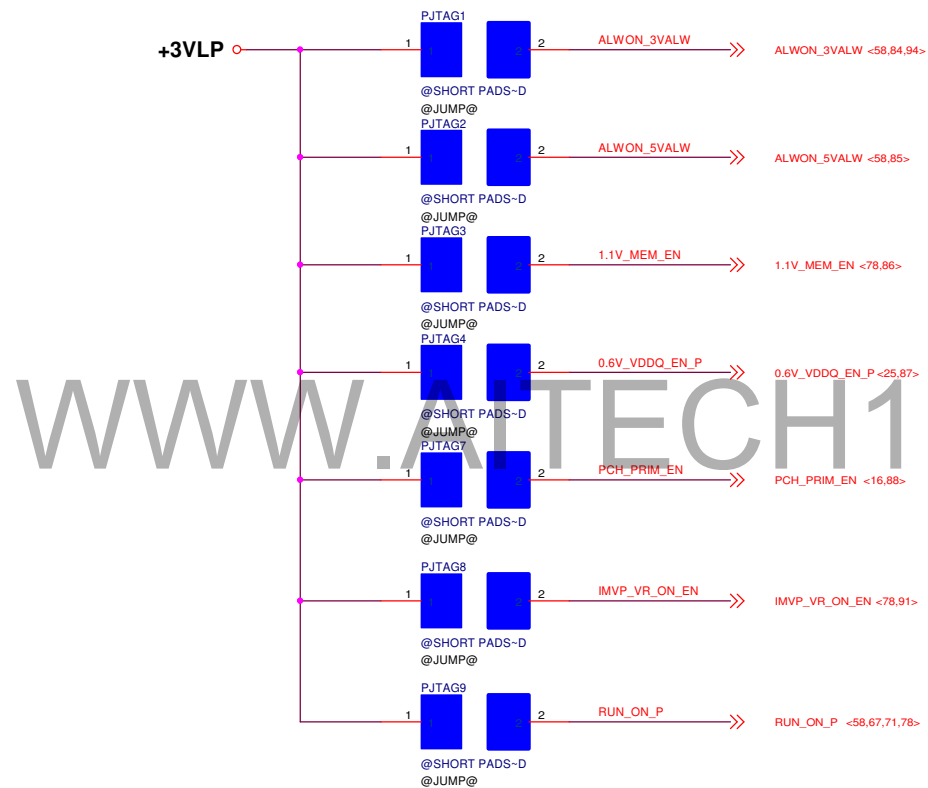
Low noise MLCC SE000015510



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Support component(37.1)





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